

## 2.64 Gbit/s Full-Duplex Serial Link Optical Piggyback Board

The GigaSTaR optical piggyback board ING\_TRF represents an easy-to-use implementation of a full-duplex GigaSTaR High-Speed link with 2.64 Gbit/s (2 x 1.32 Gbit/s) bandwidth for long distance transmission (up to 550 m) on multimode fiber. Equipped with the GigaSTaR Transmitter- and Receiver devices INGT165B/INGR165B, an optical trans-ceiver module and a few external components, the board offers all the functionality to be directly connected to a plain 2 \* 36 bit, 33 MHz parallel interface through a compact 140 pin connector. The optical signals are available at IEC-compatible standard SC Duplex connectors of the mounted Optical Transceiver Module. With the compact size of 80 x 64 mm and a variable distance of 6-14 mm to the main board, this piggyback can be easily adapted to any system environment.

The optical piggyback board can also be combined with the GigaSTaR Application Twin Kit ING\_AK2 to build a full-duplex, serial high-speed link for fast prototyping and evaluation purposes.

Technical details of the GigaSTaR devices INGT165B and INGR165B and the Application Kit ING\_AK are available in the respective product datasheets (<http://www.inova-semiconductors.com>).

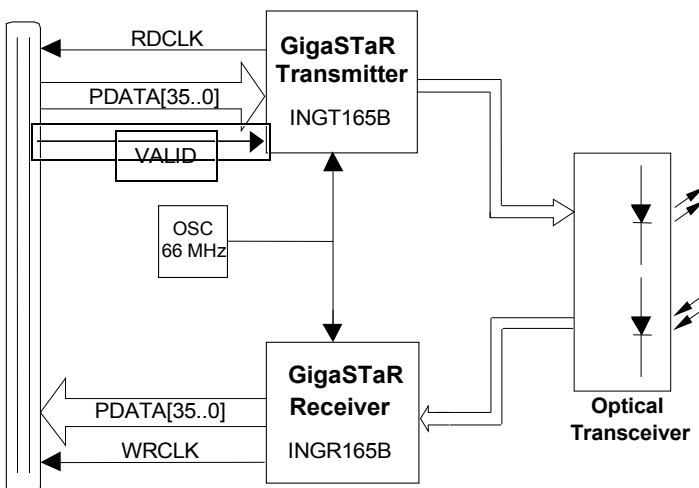


Figure 1: ING\_TRF Piggyback Board functional schematics

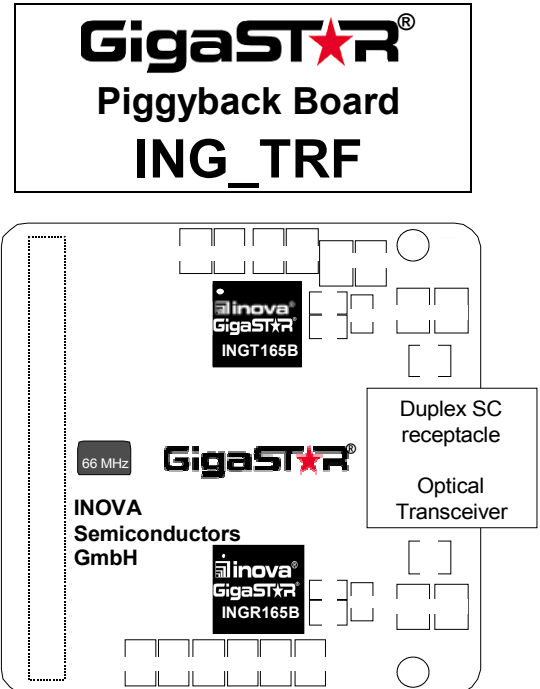


Figure 2: Topview of piggyback board

## FEATURES

- Compact size of 80 x 64 mm
- Full-duplex, 2 x 1.188 Gbit/s payload data rate (sustained)
- Parallel Tx/Rx-Interfaces (each 36 bit @ 33 MHz)
- Mounted Optical Gigabit Transceiver with IEC-compatible standard SC Duplex connectors
- 140 pin, 0.8 mm pitch free-height connector (AMP part #179029-6) for 6/10/14 mm board spacing
- On-board 66 MHz reference-clock oscillator
- Multilayer PCB board for highest EMI-immunity
- Single 3.3 V DC-supply

## 1. GigaSTaR LINK DESCRIPTION

The GigaSTaR link is designed for reliable, high-speed, low-latency data transmissions.

All functions for the data transfer management, including the high-frequency blocks, are fully integrated in the Transmitter and Receiver devices. Both devices feature a 36 bit “user-friendly” parallel interface with standard logic levels (3.3 V CMOS) for easy adaptation to any application.

The link supports an effective (sustained) data rate up to 148.5 MByte/s at the parallel interface, which translates to a serial bit stream of max. 1.188 Gbit/s (payload data rate). With 4 additional bits for link-synchronization, DC-balancing and parity check, the maximum bit rate at the serial I/Os is 1.32 Gbit/s, for an overall link efficiency of 90 percent. With only 40 ns propagation delay time each, for the Transmitter and Receiver, the typical overall latency for a GigaSTaR link with fiber-optic cable is:

$$\text{latency [ns]} = [2 \times 40 \text{ ns}] + [\text{length of fiber cable} \times 5 \text{ ns/m}] + [2 \times \text{propagation delay optical module [ns]}]$$

### 1.1 CLOCK SYSTEM

The serial bit clock frequency of 1320 MHz is generated by internal PLLs. The Transmitter and Receiver each require an external 66 MHz reference clock.

A continuous phase alignment in the Receiver ensures that the receiver’s clock is synchronous to the transmitter’s clock.

### 1.2 PARALLEL DATA FORMAT

Both the GigaSTaR Transmitter and Receiver have a synchronous 36 bit parallel interface.

The maximum frequency at this interface is 33 MHz, equivalent to a period of 30.3 ns for the WRCLK/RDCLK signals. A data word at the parallel interface consists of 36 data bits and the optional parity bit.

Additional parity I/Os allow the transfer of an optional external parity bit synchronous with the parallel data.

If an external parity bit is provided by the application at the TX\_PARITY input pin, PARGEN has to be set to ‘0’. The Transmitter will read and transfer the external parity bit at the TX\_PARITY pin and additionally will compare it with the parity bit generated internally. The TX\_PERR# signal reports any mismatch between the external parity bit and the internally generated parity bit.

If no external parity bit is available, PARGEN has to be set to ‘1’ and the Transmitter adds the internally generated parity bit to the data word. The TX\_PERR# signal is inactive when PARGEN = ‘1’.

The Receiver permanently computes the parity over each transmitted word and compares it with the transmitted parity bit. A mismatch of parity information indicates a transmission failure and the signal RX\_PERR# is asserted for one data cycle. LSYNC# is de-asserted and the Receiver starts to re-synchronize the link.

### 1.3 SERIAL DATA FORMAT

The serial data stream is DC-balanced which is performed by proprietary coding in the Transmitter device.

## 1.4 TRANSMITTER (TX) CONTROL SIGNALS

TX\_RESET# is an asynchronous active low reset signal for the Transmitter device.

TX\_PARITY is the input pin for the parity signal provided by the application.

TX\_PERR = '1' indicates that the externally provided parity bit does not match the internally generated parity bit.

TX\_LOCK = '1' indicates that the Transmitter PLL is locked. If TX\_LOCK is de-asserted the Transmitter is not ready.

PARGEN = '1' activates the internal parity generation. In this mode, the PARITY input pin is ignored. An internal parity bit is generated and transmitted.

VALID = '1' indicates to the Transmitter that data are available. With the assertion of VALID the RDCLK starts to run. PDATA[35..0] is registered at each rising edge of RDCLK. De-asserting VALID disables RDCLK and stuffing patterns are transmitted over the GigaSTaR link to maintain synchronization.

A FLAGI positive edge sets an internal flag which is transmitted at the end of the data word currently in transmission. The Receiver decodes the flag out of the serial bit-stream and toggles the level of the FLAGO output. This signal can be used to mark the end of a data frame.

## 1.5 RECEIVER (RX) CONTROL SIGNALS

RX\_RESET# is an asynchronous active low reset signal for the Receiver device.

RX\_PARITY is the output pin for the parity bit transmitted with the 36 bit data word.

RX\_PERR# is asserted for one data cycle if there is a mismatch of the transmitted and internally generated parity information. This mismatch indicates a transmission failure.

RX\_LOCK = '1' indicates that the Receiver PLL is locked. If RX\_LOCK is de-asserted, the Receiver is not ready.

EQSEL activates the internal equalizer. For optical transmissions, this feature should be activated (set to "1").

The status bit LSYNC# is asserted if the GigaSTaR Receiver has successfully synchronized to the incoming bit-stream. If the Receiver is not synchronized correctly, LSYNC# is de-asserted.

RX\_PERR#: the receiver permanently computes the parity over each transmitted word and compares it with the transmitted parity bit. A mismatch of both parity information indicates a transmission failure and the signal RX\_PERR# is asserted for one data cycle. LSYNC# is de-asserted and the Receiver starts to re-synchronize the link.

The FLAGO output provides the internal flag controlled by the FLAGI input. After reset, the state of the FLAGO output is "low".

## 1.6 GigaSTaR LINK MEDIA (COPPER OR FIBER)

The GigaSTaR Transmitter and Receiver devices are each equipped with robust high-speed interfaces that may directly connect to a fiber optic module (AC-coupling), impedance controlled cables (STP or coax) or transmission lines.

The ING\_TRF Optical Piggyback Board is configured for 62.5µm or 50µm multimode fibers with IEC-compatible standard SC Duplex or SC Simplex connectors.

## 1.7 TRANSMITTER (TX) SIGNAL TIMINGS

### 1.7.1 Data Burst Transfers

The data burst timing provides the full data rate of 148.5 MByte/s. VALID is asserted when the first data is valid at PDATA[35..0]. With every rising edge of RDCLK the PDATA inputs are registered, serialized and transmitted. VALID can remain asserted as long as new data are available.

In the timing diagram PARGEN is de-asserted and the application delivers the PARITY bit synchronously to the data word.

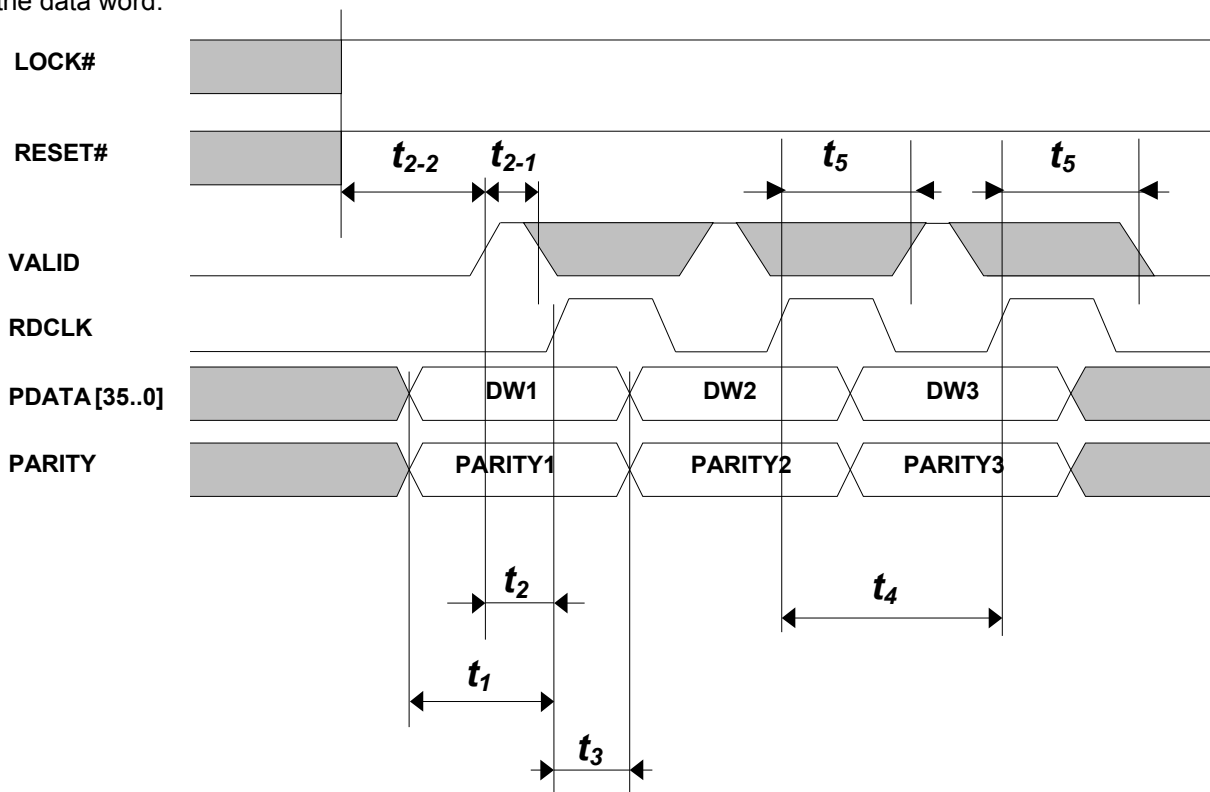


Figure 4: INGT165B Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t <sub>1</sub>	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t <sub>2</sub>	VALID active to first rising RDCLK edge	9	12	14	ns
t <sub>2-1</sub>	VALID high state	5	4		ns
t <sub>2-2</sub>	LOCK# / RESET# high state before Tx operational *	50			μs
t <sub>3</sub>	PDATA and PARITY hold time	9	6		ns
t <sub>4</sub>	RDCLK cycle time (without assertion of FLAGI)		30.3		ns
t <sub>5</sub>	Rising RDCLK edge to sampling window for VALID state (VALID=0: exit BURST mode, VALID=1: continue BURST mode)	18	20	22	ns

Note : For timings with assertion of FLAGI, please see section 3.2.5

\*A dislock pulse generates an internal transmitter reset. Therefore both signals have to be at least 50us at high state before transmitter is operational.

Table 1: INGT165B Data Burst Timing Parameters (under recommended operating conditions)

### 1.7.2 Single Word Transfers

Single Word Transfers are used to support lower data rates than the maximum parallel data rate of 148.5 MByte/s. VALID has to be de-asserted after the parallel read cycle signaled by one RDCLK pulse. Only one data word is transmitted.

In the timing diagram PARGEN is de-asserted and the application delivers the PARITY bit synchronously to the data word.

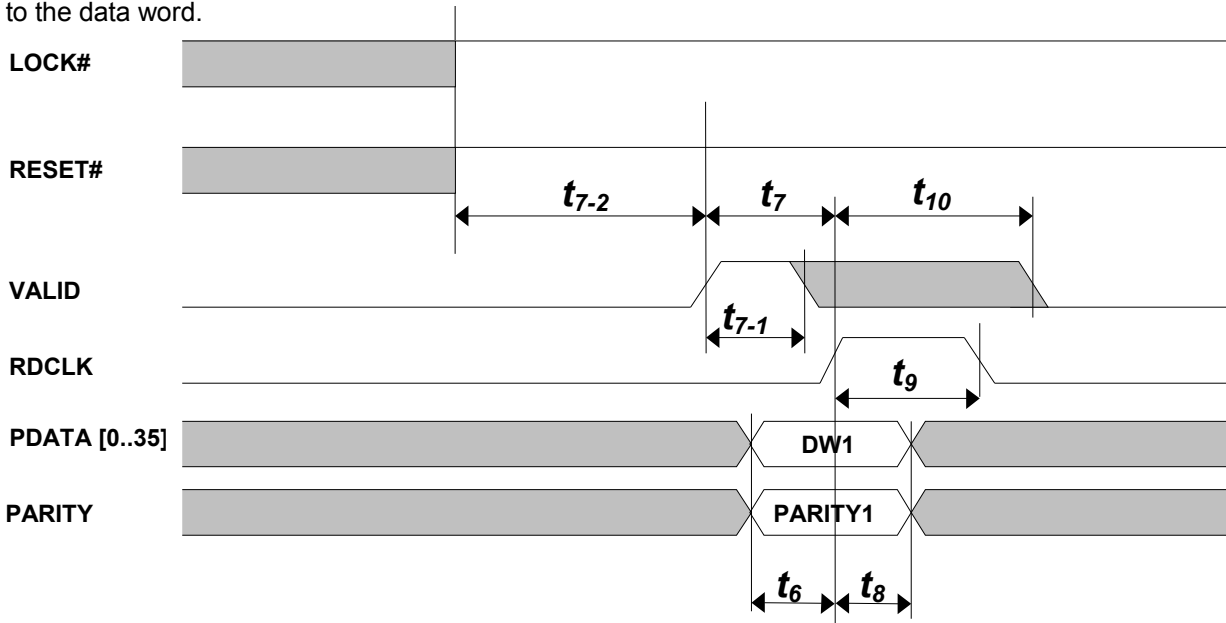


Figure 5: INGT165B Single Word Transfer Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t <sub>6</sub>	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t <sub>7</sub>	VALID active to rising RDCLK edge	9	12	14	ns
t <sub>7-1</sub>	VALID high state	5	4		ns
t <sub>7-2</sub>	LOCK# / RESET# high state before TX operational *	50			μs
t <sub>8</sub>	PDATA and PARITY hold time	9	6		ns
t <sub>9</sub>	RDCLK high state (without assertion of FLAGI)	14	15	16	ns
t <sub>10</sub>	Rising RDCLK edge to sampling window for VALID state (VALID=0: continue single word mode, VALID=1: enter BURST mode)	18	20	22	ns

Note : For timings with assertion of FLAGI, please see section 3.2.5

\* A dislock pulse generates an internal transmitter reset. Therefore both signals have to be at least 50us at high state before transmitter is operational.

Table 2: INGT165B Single Word Transfer Timing Parameters (Under recommended operating conditions)

## 1.8 RECEIVER (RX) SIGNAL TIMINGS

### 1.8.1 Data Burst Transfers

The data burst timing is used to support the full data rate of 148.5 MByte/s.

RXPDP [35..0] and RX\_PARITY are updated with each rising edge of WRCLK (see figure 5).

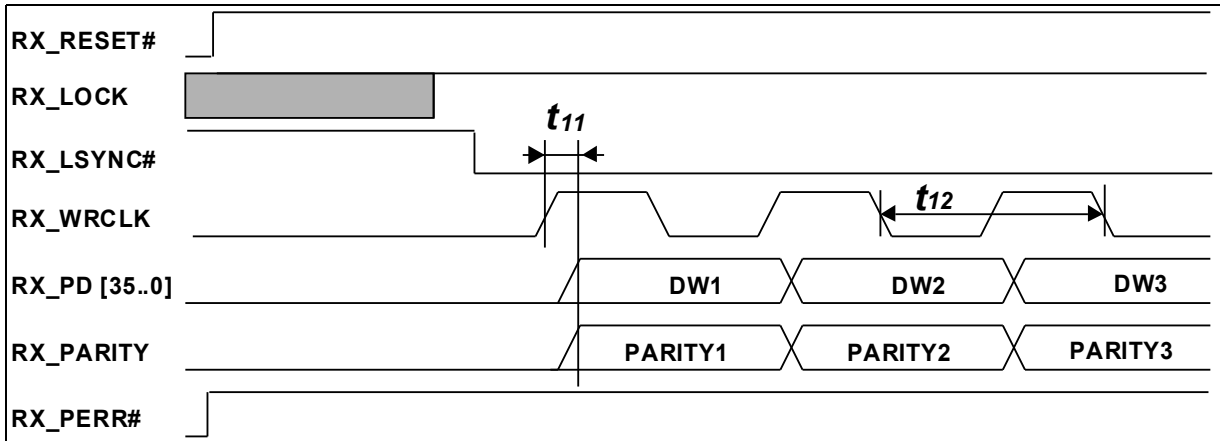


Figure 5: Receiver Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
$t_{11}$	Rising edge WRCLK to RXPd and RX_PARITY bit valid		1	4	ns
$t_{12}$	WRCLK cycle time (without assertion of FLAGI)		30.3		ns

Note: For timings with assertion of FLAGI, please see section 1.9

Table 3: Receiver Data Burst Timing Parameters (Under recommended operating conditions)

### 1.8.2 Single Word Transfers

Single Word Transfers are used to support lower data rates. Every time a new data word is received the WRCLK signal generates one clock pulse.

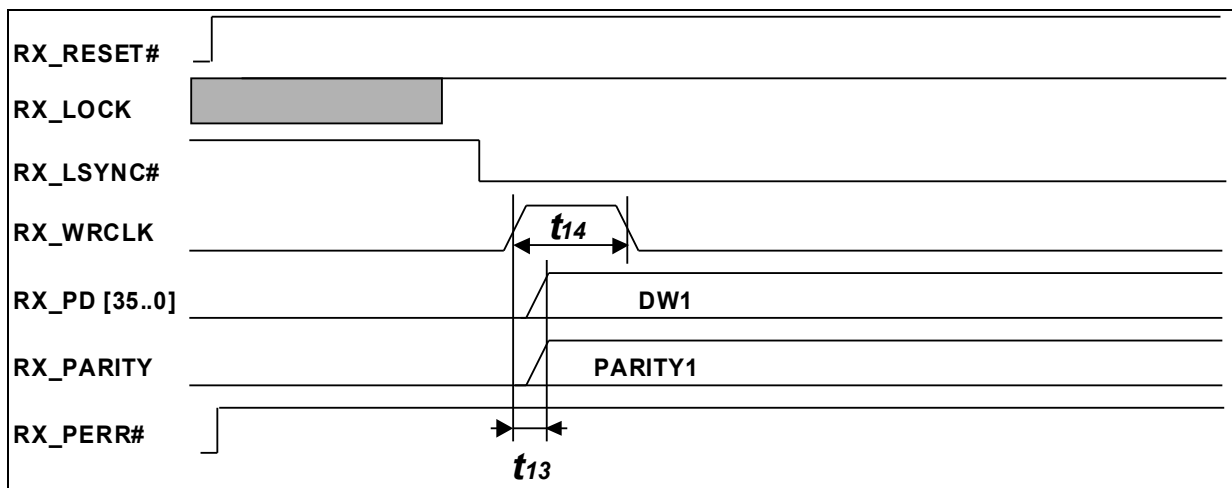


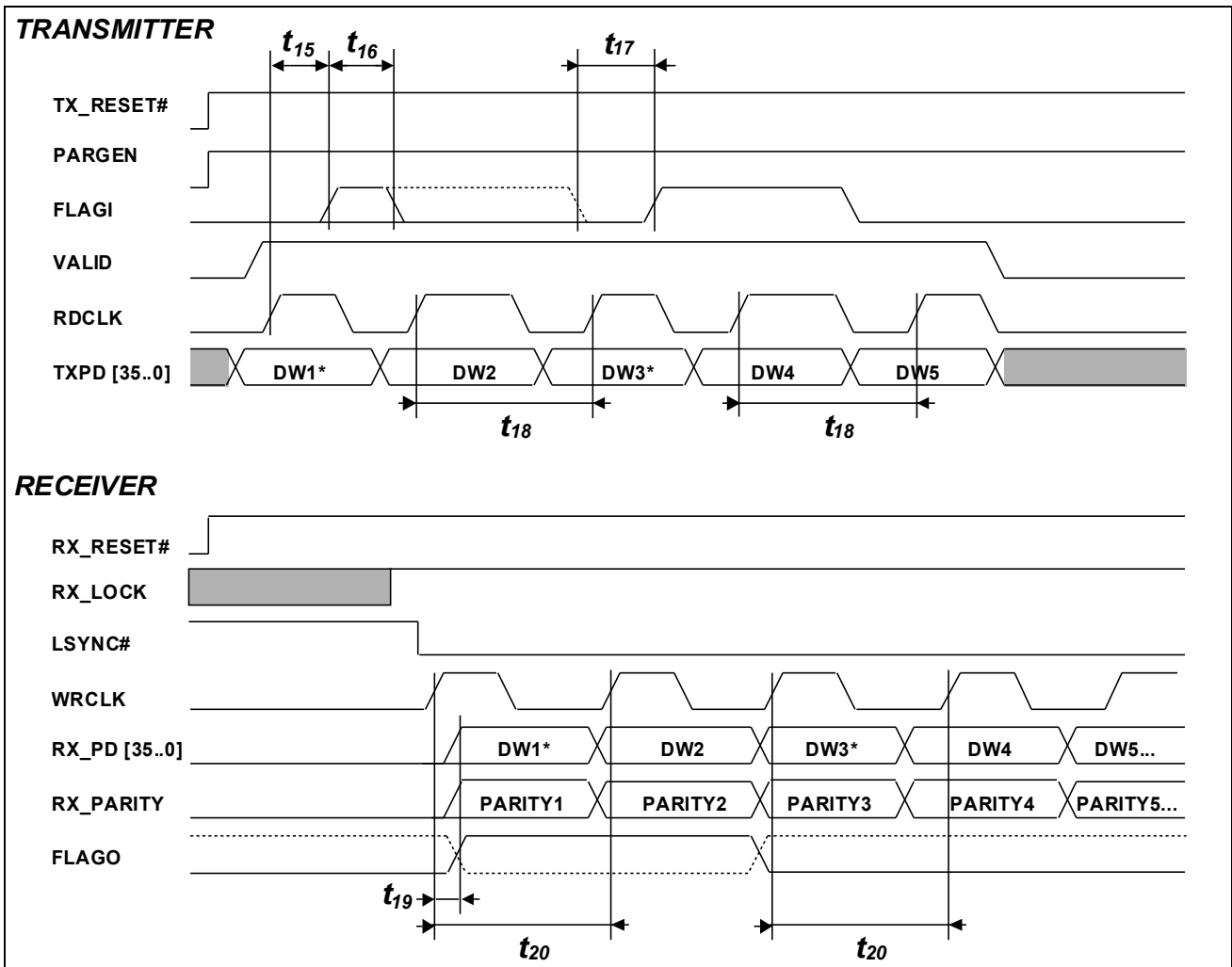
Figure 6: Receiver Single Word Transfer Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
$t_{13}$	Rising edge WRCLK to RXPd and RX_PARITY valid		1	4	ns
$t_{14}$	WRCLK high state	14	15	16	ns

Table 4: Receiver Single Word Transfer Timing Parameters (under recommended operating conditions)

### 1.9 FLAGI / FLAGO TIMING

With the FLAGI / FLAGO signals, a mechanism is provided to implement a side band signaling. Each rising edge at the Transmitter's input FLAGI toggles the FLAGO output of the Receiver. The timing diagram for the FLAGI/FLAGO signal is shown in combination with the Transmitter signals. Note that when the FLAGI signal is asserted, the following RDCLK high state time span is enlarged by app. 6 ns. At the Receiver, the WRCLK low state time span is enlarged by app. 6 ns when the FLAGO output toggles. In the diagrams below, the PARGEN is active at the Transmitter therefore no external parity is provided.



Note : \* indicates the data words [DW1, DW3] that are marked by the FLAGI signal.

Figure 7: INGT165B / INGR165B FLAGI and FLAGO Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t <sub>15</sub>	Rising edge of RDCLK to rising edge of FLAGI	0		18	ns
t <sub>16</sub>	FLAGI minimum high state		4	6	ns
t <sub>17</sub>	FLAGI minimum low state		4	6	ns
t <sub>18</sub>	RDCLK cycle time after assertion of FLAGI (one cycle only)		36		ns
t <sub>19</sub>	Rising edge of WRCLK to RXP, RX_PARITY and FLAGO valid		1	4	ns
t <sub>20</sub>	WRCLK cycle time for data word marked by FLAGO toggle		36		ns

Table 5: FLAGI and FLAGO Timing Parameters (under recommended operating conditions)

## 1.10 ERROR (REPORTING) TIMING

### 1.10.1 Parity Error (Reporting) Timing

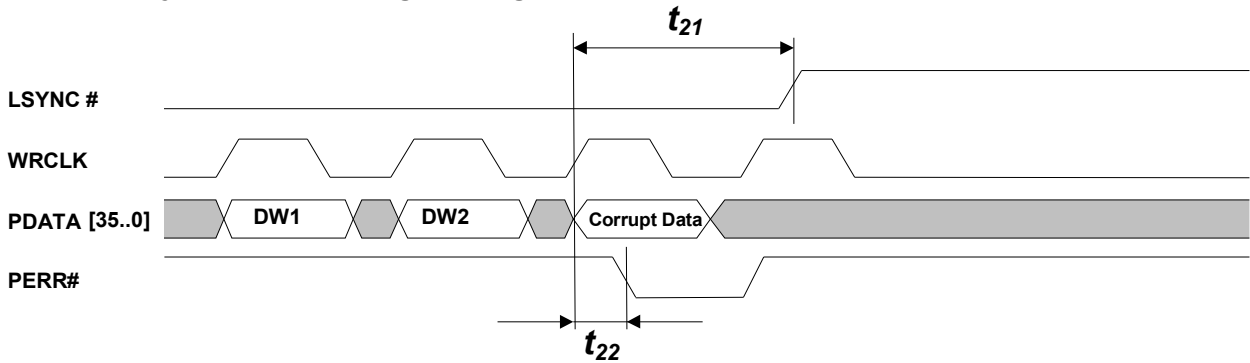


Figure 8: INGR165B Parity Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
$t_{21}$	Rising edge of WRCLK marking the corrupt data word to rising edge of LSYNC#		1	5	ns
$t_{22}$	Rising edge of WRCLK marking the corrupt data word to falling edge of PERR#		3	6	ns

Table 6: INGR165B Parity Error (reporting) timing (under recommended operating conditions)

### 1.10.2 Header/Frame Error (Reporting) Timing

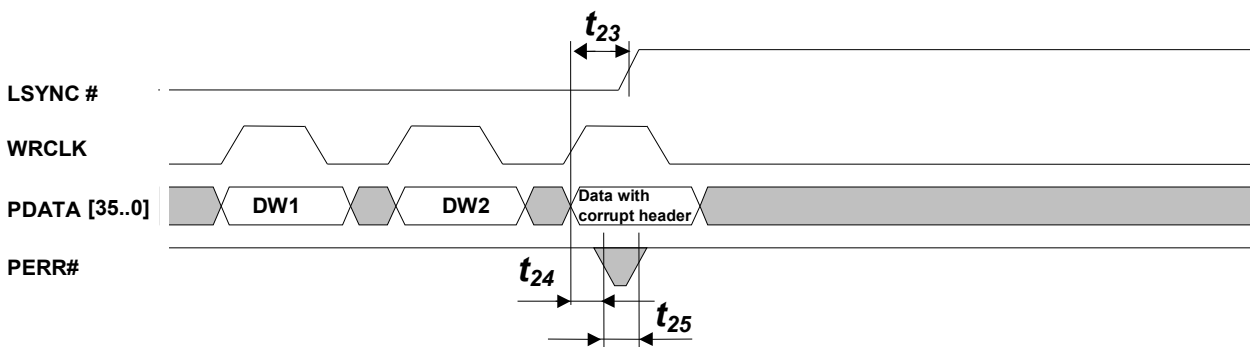


Figure 9: INGR165B Header/Frame Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
$t_{23}$	Rising edge of WRCLK marking the corrupt data header to rising edge of LSYNC#	0		13	ns
$t_{24}$	Rising edge of WRCLK marking the corrupt data header to falling edge of PERR#		1,5		ns
$t_{25}$	PERR # low state		3		ns

Table 7: Header/Frame Error (reporting) timing (under recommended operating conditions)

## 2. PIGGYBACK BOARD INTERFACE AND MOUNTING DESCRIPTION

### 2.1 AMP 140 PIN CONNECTOR DEFINITION

Pin	Signal	Pin	Signal	Pin	Signal
4	TXPD0	82	RXPD0	2	GND
6	TXPD1	84	RXPD1	11	GND
8	TXPD2	86	RXPD2	22	GND
10	TXPD3	88	RXPD3	31	GND
14	TXPD4	92	RXPD4	42	GND
16	TXPD5	94	RXPD5	51	GND
18	TXPD6	96	RXPD6	61	GND
20	TXPD7	98	RXPD7	65	GND
13	TXPD8	93	RXPD8	69	GND
15	TXPD9	95	RXPD9	73	GND
17	TXPD10	97	RXPD10	79	GND
25	TXPD11	103	RXPD11	90	GND
19	TXPD12	101	RXPD12	99	GND
24	TXPD13	102	RXPD13	110	GND
26	TXPD14	104	RXPD14	119	GND
28	TXPD15	106	RXPD15	130	GND
30	TXPD16	108	RXPD16	139	GND
27	TXPD17	105	RXPD17	1	VCC
29	TXPD18	107	RXPD18	12	VCC
34	TXPD19	112	RXPD19	21	VCC
33	TXPD20	111	RXPD20	32	VCC
36	TXPD21	114	RXPD21	41	VCC
37	TXPD22	115	RXPD22	52	VCC
38	TXPD23	116	RXPD23	62	VCC
35	TXPD24	113	RXPD24	80	VCC
39	TXPD25	117	RXPD25	89	VCC
40	TXPD26	118	RXPD26	100	VCC
44	TXPD27	122	RXPD27	109	VCC
45	TXPD28	123	RXPD28	120	VCC
54	TXPD29	132	RXPD29	129	VCC
48	TXPD30	126	RXPD30	140	VCC
53	TXPD31	131	RXPD31	23	Reserved, set to GND (*)
47	TXPD32	125	RXPD32	63	Reserved, set to VCC (*)
56	TXPD33	134	RXPD33	67	Reserved, do not connect (*)
49	TXPD34	127	RXPD34	71	Reserved, do not connect (*)
55	TXPD35	133	RXPD35	57, 59, 60	Not connected
7	TX_LOCK	87	RX_LOCK	64, 66, 68	Not connected
9	TX_PARITY	91	RX_PARITY	70, 72, 74	Not connected
58	TX_PERR#	136	RX_PERR#	75, 76, 77	Not connected
3	RX_RESET#	81	RX_RESET#	78, 124	Not connected
5	RDCLK	83	WRCLK	135, 137	Not connected
43	FLAGI	121	FLAGO	138	Not connected
46	PARGEN	85	EQSEL		Not connected
50	VALID	128	LSYNC#		(*) : These pins are reserved for optional functions

Table 8: Piggyback AMP 140 Pin Free Height Plug pin definition (AMP #179029-6)

The pin numbering definition of the AMP connector is shown in Fig. 10:

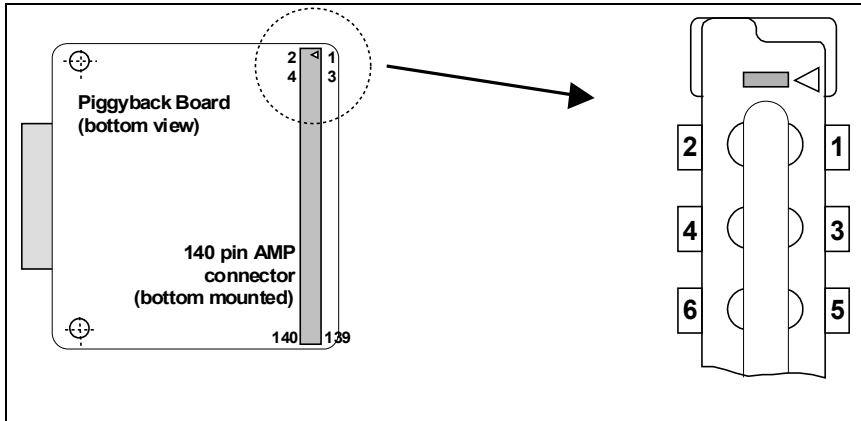


Fig. 10: Piggyback AMP 140 pin free height connector numbering

The spacing between the Piggyback Board and the main board can be 6, 10 or 14 mm with the respective AMP free height receptacle (AMP part numbers AMP177983-6/AMP 5-179009-6/AMP 5-179010-6).

## 2.2 OPTICAL I/Os

The IEC-compatible standard SC Duplex connectors are located as shown in figure 11:

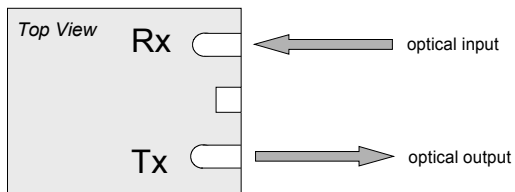


Fig. 11: Optical Transceiver Module

### 3. OPTICAL PIGGYBACK BOARD SPECIFICATION

#### 3.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors may not be held liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above those indicated in the recommended operating conditions is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V <sub>CC</sub>	-0.5	+4.2	V	
Input Voltage	V <sub>IN</sub>	-0.5	V <sub>CC</sub> +0.5	V	
I/O Current (DC or transient any pin)	I <sub>D</sub>	-20	+20	mA	
Ambient Temperature (under bias)	T <sub>A</sub>	-40	+70	° C	
Storage Temperature	T <sub>stg</sub>	-40	+85	° C	
Static Discharge Voltage (AMP connector pins)	V <sub>SDAMP</sub>		± 2000	V	Human Body Model

Table 9: Absolute Maximum Ratings

#### 3.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V <sub>CC</sub>	+3.15	+3.45	V	
Input Voltage	V <sub>IN</sub>	0	V <sub>CC</sub>	V	V <sub>CC</sub> = 3.3V ± 0.15V
Ambient Temperature	T <sub>a</sub>	-40	+70	° C	Air flow >= 250 LFPM

Table 10: Recommended Operating Conditions

Please note: It is recommended to avoid transmitting of parallel data words (TXPD[35..0]) that contain long sequences of logic 0 or 1 bits. This leads into long OFF- or ON-times for the laser in the optical transceiver and can decrease transmission performance.

#### 3.3 ELECTRICAL SPECIFICATION

##### 3.3.1 DC – Characteristics (under recommended operating conditions)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input High Voltage	V <sub>IH</sub>		2.6			V
Input Low Voltage	V <sub>IL</sub>				0.7	V
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>CC</sub>	-10		10	µA
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> = 0 V	-10		-150	µA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.5 mA	0,95 V <sub>CC</sub>			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.5 mA			0,05 V <sub>CC</sub>	V
LOCK Output High Current	V <sub>LH</sub>	I <sub>OH</sub> = -0.5 mA	0,9 V <sub>CC</sub>			mA
LOCK Output Low Current	V <sub>LL</sub>	I <sub>OL</sub> = 1.5 mA			0,1 V <sub>CC</sub>	mA
Supply Current	I <sub>CC</sub>	Max. data transmission rate		830	1030	mA
Power Dissipation	P <sub>D</sub>	Max. data transmission rate		2,74	3,34	W

Table 11: DC – Characteristics

### 3.3.2 AC- Characteristics (under recommended operating conditions)

Parameter	Description	Min.	Typ.	Max.	Unit
t <sub>1</sub>	Setup time TXPD and TX_PARITY to RDCLK rising edge	9	6		ns
t <sub>2</sub>	VALID active to first rising RDCLK edge	9	12	14	ns
t <sub>2-1</sub>	VALID high state	5	4		ns
t <sub>2-2</sub>	LOCK# / RESET# high state before Tx operational	50			μs
t <sub>3</sub>	TXPD and TX_PARITY hold time	9	6		ns
t <sub>4</sub>	RDCLK cycle time (without assertion of FLAGI)		30.3		ns
t <sub>5</sub>	Rising RDCLK edge to sampling window for VALID state (VALID=0: exit BURST mode, VALID=1: continue BURST mode)	18	20	22	ns
t <sub>6</sub>	Setup time TXPD and TX_PARITY to RDCLK rising edge	9	6		ns
t <sub>7</sub>	VALID active to rising RDCLK edge	9	12	14	ns
t <sub>7-1</sub>	VALID high state	5	4		ns
t <sub>7-2</sub>	LOCK# / RESET# high state before Tx operational	50			μs
t <sub>8</sub>	TXPD and TX_PARITY hold time	9	6		ns
t <sub>9</sub>	RDCLK high state (without assertion of FLAGI)	14	15	16	ns
t <sub>10</sub>	Rising RDCLK edge to sampling window for VALID state (VALID=0: continue single word mode, VALID=1: enter BURST mode)	18	20	22	ns
t <sub>11</sub>	Rising edge WRCLK to RXPD and RX_PARITY bit valid		1	4	ns
t <sub>12</sub>	WRCLK cycle time (without assertion of FLAGI)		30.3		ns
t <sub>13</sub>	Rising edge WRCLK to RXPD and RX_PARITY valid		1	4	ns
t <sub>14</sub>	WRCLK high state	14	15	16	ns
t <sub>15</sub>	Rising edge of RDCLK to rising edge of FLAGI	0		18	ns
t <sub>16</sub>	FLAGI minimum high state		4	6	ns
t <sub>17</sub>	FLAGI minimum low state		4	6	ns
t <sub>18</sub>	RDCLK cycle time after assertion of FLAGI (one cycle only)		36		ns
t <sub>19</sub>	Rising edge of WRCLK to RXPD, RX_PARITY and FLAGI valid		1	4	ns
t <sub>20</sub>	WRCLK cycle time for data word marked by FLAGO toggle		36		ns
t <sub>21</sub>	Rising edge of WRCLK after the corrupt data word to rising edge of LSYNC#		1	5	ns
t <sub>22</sub>	Rising edge of WRCLK marking the corrupt data word to falling edge of RX_PERR#		3	6	ns
t <sub>23</sub>	Rising edge of WRCLK marking the corrupt data header to rising edge of LSYNC#	0		13	ns
t <sub>24</sub>	Rising edge of WRCLK marking the corrupt data header to falling edge of RX_PERR#		1,5		ns
t <sub>25</sub>	RX_PERR # low state		3		ns

Table 12: Transmitter and Receiver Timing Parameters (under recommended operating conditions)

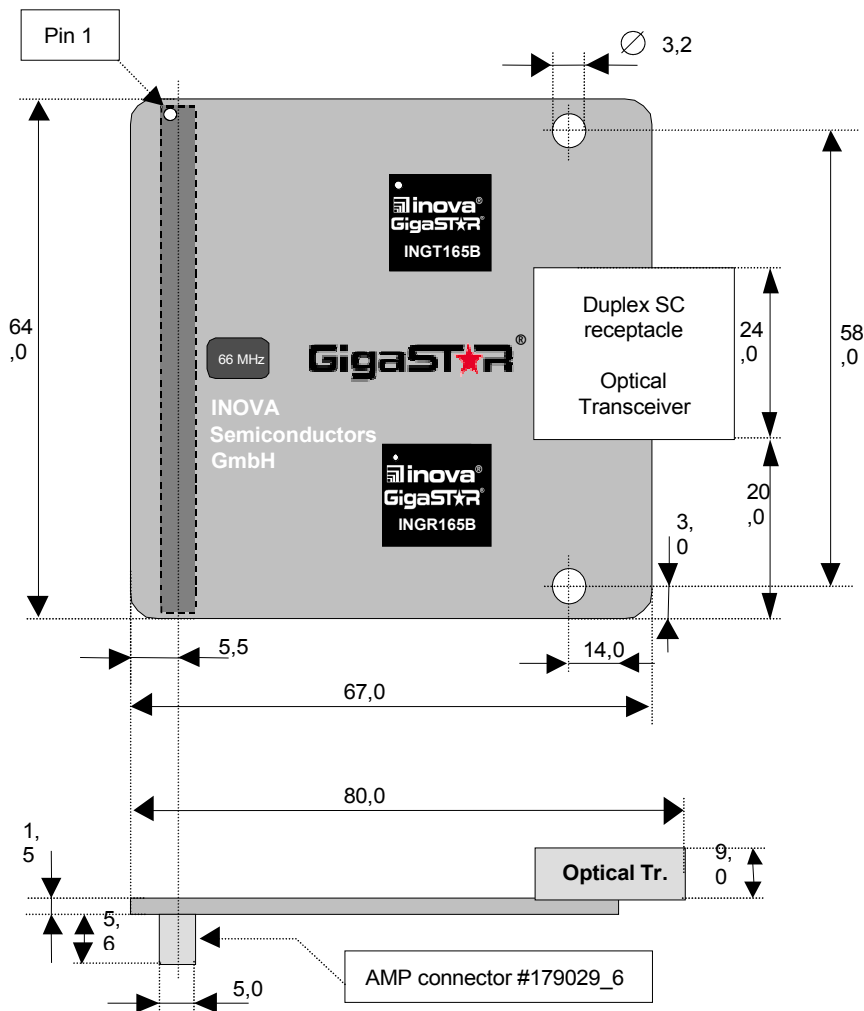
### 3.4 OPTICAL TRANSCEIVER

Part nbr. of the Optical Transceiver Module:

- V23826-K305-C373 (FINISAR), or
- M3-125-SAT (OPTICIS)

Due to individual shut off conditions of the fiber transmitters after continuous “zero” or “one”, a minimum bandwidth (e.g. 140 Mbit/s) has to be maintained. For details please see their respective datasheets.

### 3.5 PIGGYBACK BOARD DIMENSIONS



All dimensions are given in millimeters

Figure 12: Top and side view of the Piggyback Board ING\_TRF

### 3.6 HANDLING PRECAUTIONS

Handling precautions are:

1. The maximum ratings may not be exceeded at any time.
2. Precautions have to be taken against exposure of the board terminals to electrostatic discharge stress.
3. Mounting and dismounting of the piggyback board should be performed with care and the mounting/dismounting cycles should be limited in order to avoid AMP connector wearout.
4. For ambient operating temperatures above +40° C, an air flow with  $\geq 250$  LFPM has to be provided.

### 3.7 ORDERING CODE AND PRODUCTION STATUS INFORMATION

Ordering Code	Delivery option	Production Status
ING_TRF	Optical Piggyback Board with IEC-compatible standard SC Duplex connectors	Released to full production

Table 13: Product Availability

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