



Xilinx APIX Transmitter



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Product Specification



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AllianceCORE Facts	
Provided with Core	
Documentation	datasheet
Design File Formats	NGC netlist
Constraints Files	TAPIX_CORE.ucf
Verification	Hardware Verification
Instantiation Templates	Verilog
Reference Designs & Application Notes	none
Additional Items	none
Simulation Tool Used	
none	
Support	
Support provided by INOVA Semiconductors GmbH	

Features

APIX1 Core Function Transmission of 24 Bit video data. Full duplex sideband communication, utilizes XILINX MGT serial high speed I/O's Available under the SignOnce IP Licensing agreement supports Xilinx Spartan6™ FPGA's

Applications

Central Infotainment Displays (CID)
Instrument Cluster
Rear-Seat Entertainment Systems
Head-Up Displays
Automotive Driver Assistance
Diagnostic Systems
Camera Systems
Medical Equipment

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM (RAMB8BW ^{ER})	MULT/ DSP48/E	DCM / CMT	MGT	Design Tools
Spartan®-6	XC6SLX45T-3	125	451	55	6	5	0	2	1	ISE® 12.3

Notes:

- 1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
- 2) Assuming all core I/Os and clocks are routed off-chip

General Description

XILINX APIX Transmitter provides all transmitter functions of a high-speed full duplex differential serial APIX communication link utilizing dedicated XILINX MGT high speed serial I/O's with adjustable drive current and pre-emphasis.

The XILINX APIX Transmitter video interface supports parallel video data format with four different color depths. In addition to the up to 24 bit pixel data interface transmission of three control signals, Hsync, Vsync and Data Enable is implemented.

XILINX APIX Transmitter provides a transparent bi-directional sideband interface.

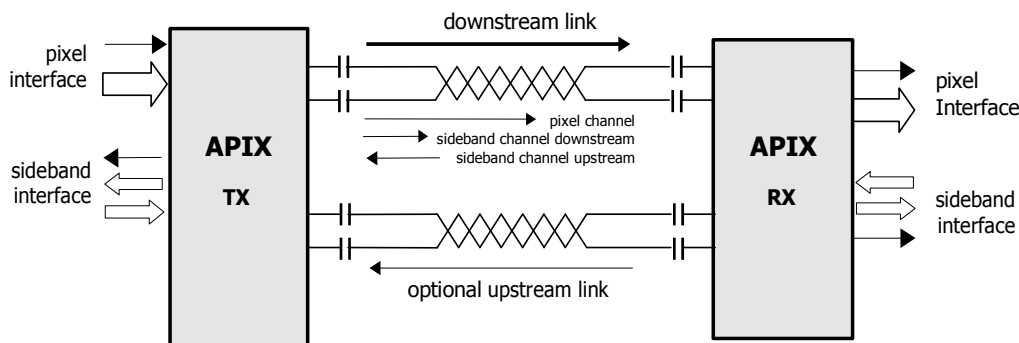


Figure 1 : APIX system overview

Functional Description

Serial interface

downstream link running at 1Gbit/s utilizing XILINX high speed MGT I/O's

Optional upstream link running at 62.5Mbit/s for sideband communication

Video interface

Transmission of parallel RGB video data and control signals with 10, 12, 18 or 24 bit widths

Sideband interface

Transmission of bi-directional sideband data (2 Bit in each direction)

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Signal	Signal Direction	Description
reset_n_i	Input	core reset request
disable_tapix_i	Input	disable APIX core
ext_ref_clk_p_i	Input	differential MGT reference clock input (75MHz)
ext_ref_clk_n_i	Input	differential MGT reference clock input (75MHz)
tx_sdout_p_o	Output	differential APIX serial output data stream (MGT)
tx_sdout_n_o	Output	differential APIX serial output data stream (MGT)
tx_sdin_p_i	Input	differential APIX serial input data stream
tx_sdin_n_i	Input	differential APIX serial input data stream
tx_nom_driver_i [3:0]	Input	control of nominal current of APIX serial output data stream
tx_preemphasis_i [2:0]	Input	control of pre-emphasis current of APIX serial output data stream
cfg_pxdata_width_i [1:0]	Input	selects the width of pixel data to be transmitted 00 – 10 Bit 01 – 12 Bit 10 – 18 Bit 11 – 24 Bit
cfg_px_in_ctrl_i [1:0]	Input	selects transmission of pixel control signals 00 – never 01 – unused 10 – on even pixels 11 – on every pixel
px_data_i [23:0]	Input	pixel data to be transmitted
px_ctrl_i [2:0]	Input	pixel control data to be transmitted
px_clk_i	Input	pixel clock input
sbdown_data_i [1:0]	Input	downstream sideband data input
sbup_data_o [1:0]	Output	upstream sideband data output
sbup_data_valid_o	Output	upstream sideband data valid output
sbup_aligned_o	Output	indicates APIX serial upstream synchronization
serial_pll_locked_o	Output	indicates status of MGT transceiver PLL
core_pll_locked_o	Output	indicates status of APIX core clock PLL

Table 2: Core I/O Signals.

Verification Methods

The APIX Transmitter core has been verified through extensive simulation and hardware verification.

Recommended Design Experience

The users should have experience in the following areas:

- Synchronous digital circuit design
- XILINX ISE tools

The user must be familiar with HDL design methodology as well as instantiation of XILINX netlists in a hierarchical design environment.

Ordering Information

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