



Embedded APIX Transmitter



February 26, 2010

Product Specification Preliminary



INOVA Semiconductors GmbH

Grafinger Straße 26
DE-81761 Munich, Germany
Phone: +49-89-457475-60
Fax: +49-89-457475-88
E-mail: info@inova-semiconductors.de
URL: www.inova-semiconductors.de

Features

- Complete APIX Function and ASHELL implementation
- Transmission of RGB video data
- Implementation of full duplex Sideband Communication via ASHELL
- Transmission link status information and simple error statistics
- Error control (optional)
 - Window based ACK protocol to manage bit errors occurring during serial transmission over the wire-based APIX link.
- Available under the SignOnce IP Licensing agreement
- Supports Virtex-5™ Xilinx Spartan-6™ FPGA's

AllianceCORE Facts

| Provided with Core | |
|---|-----------------------------|
| Documentation | User Guide |
| Design File Formats | Encrypted NGC netlist |
| Constraints Files | TAPIX_embedded_internal.ucf |
| Verification | Test Bench, Test Vectors |
| Instantiation Templates | VHDL |
| Reference Designs & Application Notes | none |
| Additional Items | none |
| Simulation Tool Used | |
| ModelTech's Modelsim | |
| Support | |
| Support provided by INOVA Semiconductors GmbH | |

Applications

- Central Infotainment Displays (CID)
- Automotive Dashboards
- Rear-Seat Entertainment Systems
- Head-Up Displays
- Automotive Driver Assistance
- Diagnostic Systems
- Camera Systems
- Medical Equipment

Table 1: Example Implementation Statistics for Xilinx® FPGAs

| Family | Example Device | Fmax (MHz) | Slices ¹ | IOB ² | GCLK | BRAM | MULT/DSP48/E | DCM / CMT | MGT | Design Tools |
|-------------|----------------|------------|---------------------|------------------|----------------|------|--------------|-----------|-----|--------------|
| Virtex®-5 | XC5VFX70T | 125 | | 276 | 11 | 0 | 0 | 1 | 1 | ISE® 11.3 |
| Spartan® -6 | XC6SLX45T | 125 | | 276 | 8 | 0 | 0 | 2 | 1 | ISE® 11.3 |
| Spartan® -6 | XC6SLX45T | 125 | | 184 ³ | 6 ³ | 0 | 0 | 2 | 1 | ISE® 11.3 |

Notes:

- 1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
- 2) Assuming all core I/Os and clocks are routed off-chip
- 3) Values for APIX Core without ASHELL

February 26, 2010

PB_TAPIX_03

General Description

Embedded APIX Transmitter is part of a high-speed full duplex differential serial APIX communication link. Access is provided to a configurable parallel video interface and to the APIX Automotive AShell.

The Embedded APIX Transmitter video interface supports parallel RGB (YCbCr) format with four different color depths. In addition to the up to 24 bit pixel data interface three control signals, Hsync, Vsync and Data Enable, are implemented. The active edge of the pixel clock input is programmable.

Parallel video data can be transmitted by the Embedded APIX Transmitter to a corresponding APIX Receiver interface.

APIX Automotive Shell is a communication protocol defined by INOVA Semiconductors to ensure secure data transaction over the full duplex serial APIX link.

An application and an Embedded APIX Transmitter with AShell form a stacked bidirectional wire-based communication system with a corresponding AShell on the Receiver side (Figure 1). As part of this communication stack, AShell provides two interfaces for the exchange of messages from local to a remote island or vice versa. This encapsulation provides for higher levels of abstraction and supports a functional layered architecture of the communication system.

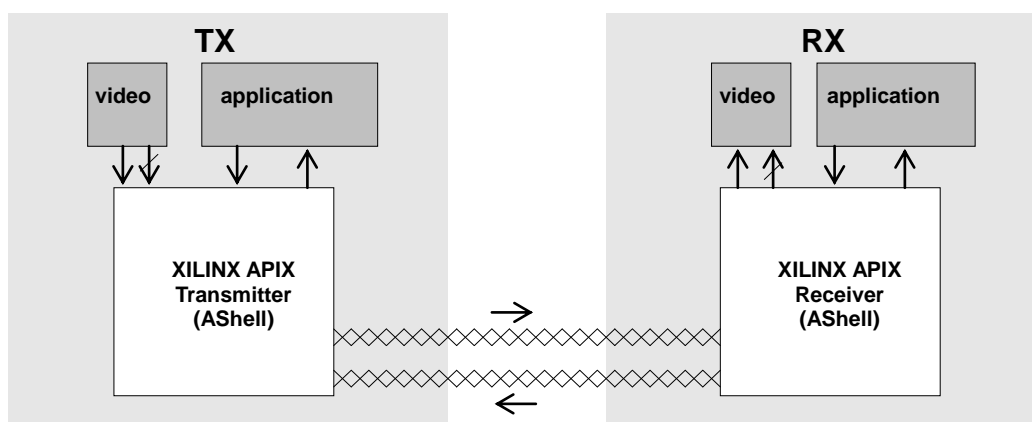


Figure 1 : APIX based communication system

Functional Description

APIX video interface

- Transmission of parallel RGB video data and control signals with different bit widths and selectable pixel clock edge

ASHELL interface

- Transaction framing and de-framing
Payload data sinked to or sourced by an application is compiled to or extracted from PDUs (transactions) exchanged as protocol entities between local and remote AShell.
- Data integrity control
AShell implements a CRC-24 polynomial to detect most transmission errors. Only valid transactions are offered to the application.
- Error control (optional)
AShell implements a window based ACK protocol to manage bit errors occurring during serial transmission over the wire-based APIX link
- Status report
Information about the transmission status as well as error statistics are collected and presented to the application at the interface.
- ASHELL can be disabled to save FPGA slices

APIX serial interface

- The APIX serial interface is utilizing the XILINX MGT transceiver outputs for optimum performance

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

| Signal | Signal Direction | Description |
|--------------------------|------------------|--|
| ap_clk | Input | Application clock |
| ap_reset_n | Input | Application reset request |
| ap_restart | Input | AShell is reinitialized and alignment restarts |
| ap_data_in[55:0] | Input | Application outbound transaction data |
| ap_data_in_valid | Input | Signalizes new transaction request to AShell |
| tx_config | Input | Forces reconfiguration of TAPIX AShell |
| config_byte_1[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_2[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_3[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_4[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_5[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_6[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_7[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_8[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_9[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_10[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_11[7:0] | Input | TAPIX embedded configuration vector |
| config_byte_shell_1[7:0] | Input | TAPIX embedded AShell configuration vector |
| config_byte_shell_2[7:0] | Input | TAPIX embedded AShell configuration vector |
| config_byte_shell_3[7:0] | Input | TAPIX embedded AShell configuration vector |
| config_byte_shell_4[7:0] | Input | TAPIX embedded AShell configuration vector |
| sbdwn_data_gpio_in | Input | Interface to external APIX device |
| sbdwn_clk_gpio_in | Input | Interface to external APIX device |
| sbup_data_gpio_in | Input | Interface to external APIX device |

Table 2: Core I/O Signals.

| Signal | Signal Direction | Description |
|---------------------------|------------------|---|
| ap_data_out[55:0] | Output | Application inbound transaction data |
| ap_data_out_valid | Output | Flags 'ap_data_out' as valid |
| ap_strobe | Output | Handshake signal. Indicates that AShell reads applications data |
| fatal_error | Output | Status output signal |
| crc_error | Output | Status output signal. Indicates CRC error in inbound data |
| tx_up_crc_error_cnt[7:0] | Output | Status output signal |
| operational | Output | Status output signal |
| ready_for_data | Output | Status output signal |
| outbound_handshake | Output | Status output signal |
| inbound_handshake | Output | Status output signal |
| crc_timeout | Output | Status output signal |
| protocol_error | Output | Status output signal |
| remote_ashell_restarted | Output | Status output signal |
| tx_up_sync_loss_cnt [7:0] | Output | Status output signal |
| tx_pll_good | Output | MGT PLL status signal |
| tx_up_ready | Output | Status output signal |
| sbdow_data_gpio_out | Output | Interface to external APIX device |
| sbdow_clk_gpio_out | Output | Interface to external APIX device |
| sbup_data_gpio_out | Output | Interface to external APIX device |
| sbup_clk_gpio_out | Output | Interface to external APIX device |
| px_data [23:0] | Input | Video interface RGB inputs |
| px_ctrl [2:0] | Input | Video interface control inputs |
| px_clk | Input | Video interface clock input |
| ext_ref_clk_p_pad | Input | Reference clock for MGT I/O's |
| ext_ref_clk_n_pad | Input | Reference clock for MGT I/O's |
| TX_SDOUT_p_pad | Output | TAPIX embedded serial differential MGT output (downstream) |
| TX_SDOUT_n_pad | Output | TAPIX embedded serial differential MGT output (downstream) |
| TX_SDIN_p_pad | Input | TAPIX embedded serial differential inputs (upstream) |
| TX_SDIN_n_pad | Input | TAPIX embedded serial differential inputs (upstream) |

Table 2: Core I/O Signals.

Verification Methods

The Embedded APIX Transmitter core has been verified through extensive simulation and rigorous code coverage measurements as well as hardware verification.

Recommended Design Experience

The users should have experience in the following areas:

- Synchronous digital circuit design
- XILINX ISE tools

The user must be familiar with HDL design methodology as well as instantiation of XILINX netlists in a hierarchical design environment.

Ordering Information

This product is available directly from Xilinx Alliance Program member INOVA Semiconductors GmbH under the terms of the SignOnce IP License. Please contact INOVA Semiconductors GmbH for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact INOVA Semiconductors GmbH

URL: www.inova-semiconductors.de/signonce

or visit the web:

Email: commonlicense@xilinx.com

URL: www.xilinx.com/ipcenter/signonce

This publication has been carefully checked for accuracy. However, INOVA Semiconductors GmbH does not assume any responsibility for the contents or use of any product described herein. INOVA Semiconductors GmbH reserves the right to make any changes to products without further notice. Our customers should ensure that they take appropriate action so that their use of our products does not infringe upon any patents. INOVA Semiconductors GmbH products are not intended for use in life support applications. Use of the INOVA Semiconductors GmbH products in such appliances is prohibited without written GmbH approval.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com