May 2009
Revision 1.2

APIX – Evaluation Kit, Revision 3.0

The APIX Evaluation Kit is designed to evaluate the performance and all configuration options of the INAP125T24 and INAP125R24 devices. A graphical PC user interface allows to set all registers as well as pre-emphasis and nominal current settings. Optimized for low EMI, the boards may also be used for emission and immunity tests.

Hardware Features:

- Access to the APIX parallel pixel interface via ribbon cable connectors
- Control of the physical layer settings (amplitude, pre-emphasis) via digital potentiometers
- APIX configuration via EEPROM
- EEPROM programming support via PC and µC
- Real-time video data test pattern generation and verification for bit error testing
- Real-time side-band data test pattern generation and verification for bit error testing
- Control of all board functions via RS232 communication

User interface software features:

- Control of all hardware board functions (reset, test pattern generation, physical layer set-up)
- Automatic bit error testing to verify and optimize physical layer settings
- Convenient control of all APIX configuration options

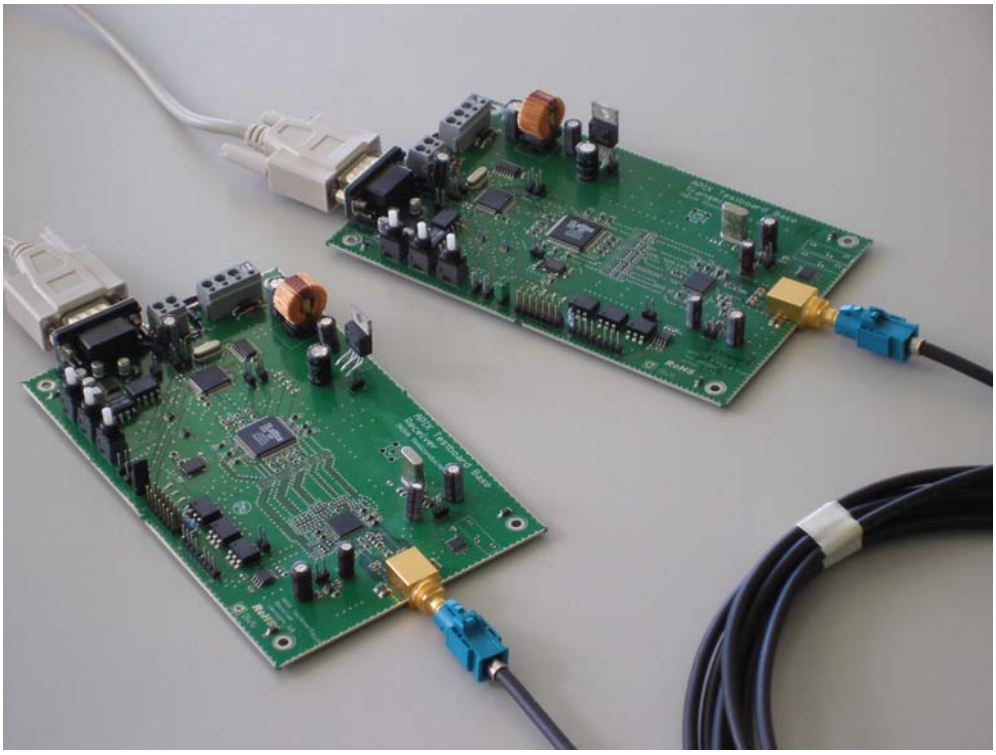

Figure 1: APIX Evaluation Kit

1.0 Overview

The APIX link transmits uncompressed pixel data with a sustained and resolution-independent link data rate of either 1 GBit/s or 500 MBit/s over one single pair of STP copper cable. In addition to the pixel data, bidirectional sideband control data can be transmitted over the same or a separate pair of wires.
The link supports distances of up to +15m (1 GBit/s mode) and up to +40m (500 MBit/s mode) depending on the output settings (current, pre-emphasis) and the cable properties.
Optimized for low EMI, the APIX link is dedicated for point-to-point applications within vehicles. The highly integrated architecture allows the implementation of video and audio links in applications like central information displays, dashboard and head-up displays, but also camera links as part of driver assistance systems requiring real-time digital video streams.

The APIX Evaluation Kit is designed to assist the customer in the first evaluation phase. It can be used further as a design and layout example to support customer-specific designs.

It consists of one transmitter board (TX), one receiver board (RX), one 5,0 m quad STP cable for the high-speed communication and two RS232 cables for PC communication.

The PC Software is designed to work with both boards, to be able to test various parameters on the complete link, or with only one board (TX or RX) to act as counterpart for your application.

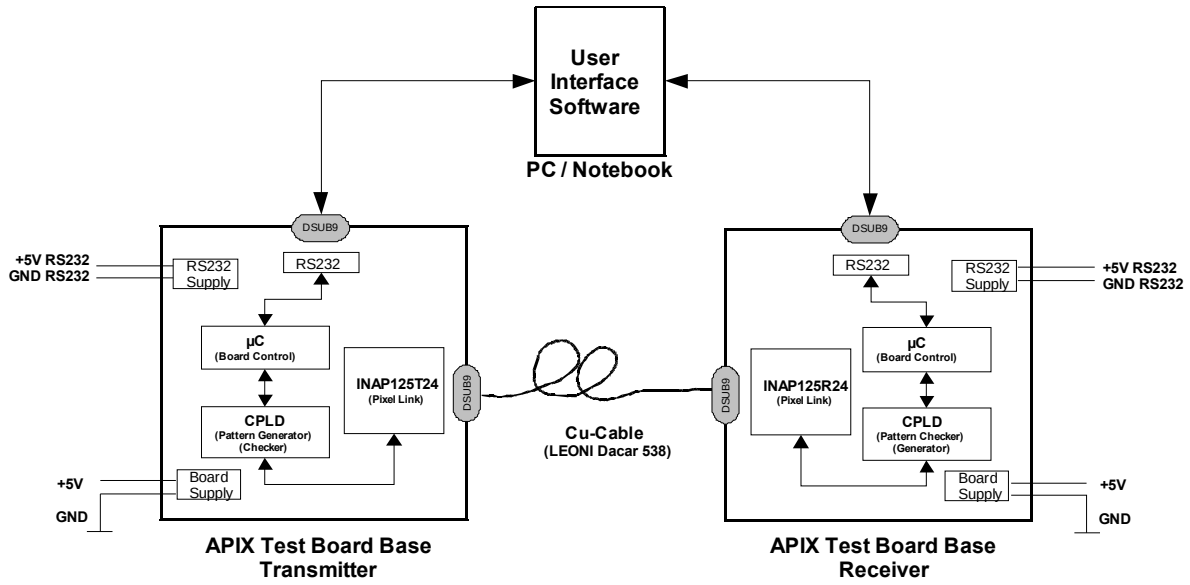

Figure 2: APIX Evaluation Kit setup

2.0 Hardware Description

2.1 Common Function Blocks on Transmitter and Receiver Board

2.1.1 Layout of Functional Blocks

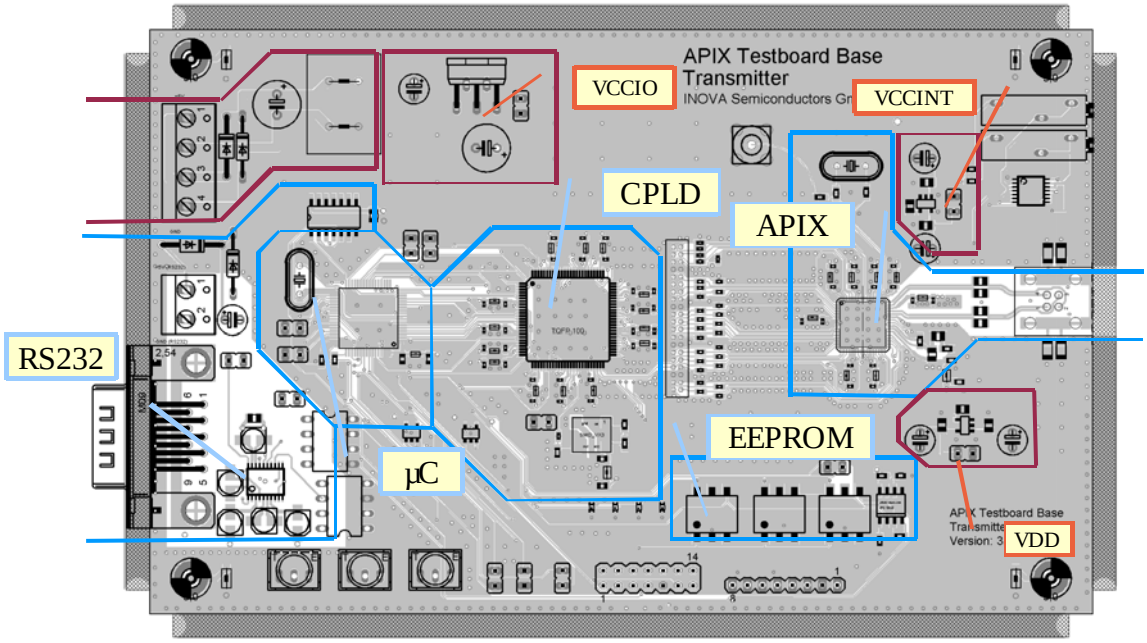

Figure 3: TX Board Functional Blocks

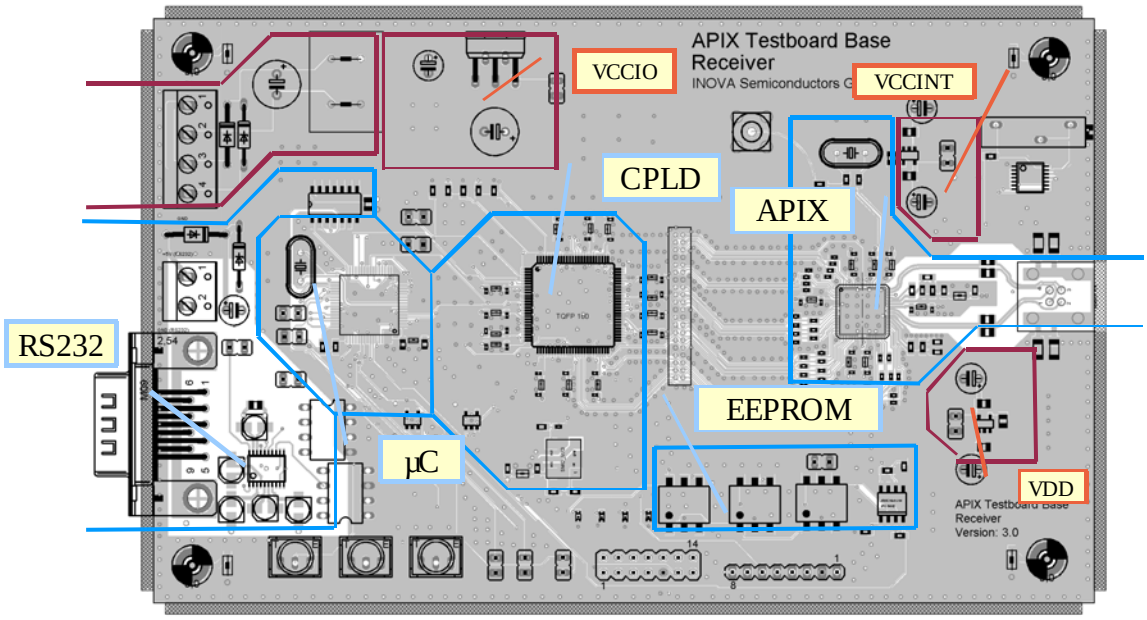

Figure 4: Rx Board Functional Blocks

2.1.2 RS232

The RS232 interface implements the communication between the evaluation board and the user interface software running on a PC or laptop. The interface is optically decoupled from the application board. It has a separate power supply (connector X4). To support extremely low-noise EMV measurements, the interface can be completely deactivated by JP13.

2.1.3 Board Controller

All board functions can be controlled via a microcontroller (MSP430F168). The µC implements the RS232 communication in the user interface software. It communicates with the CPLD via a parallel register bus to set up and activate functions which are implemented in the CPLD. It obtains status and error information from APIX and CPLD. It moreover controls the physical layer settings of APIX (nominal and pre-emphasis current) via digital potentiometers.

For a convenient configuration of APIX, the APIX configuration EEPROM can be programmed through the µC.

2.1.4 CPLD

The CPLD mainly serves to generate and check test data for the pixel and side-band data interface. In addition, the CPLD preprocesses status and error data of the APIX devices.

The format of the pixel data can be freely defined (visible data area, blanking). Different pixel clock frequencies ranging from some MHz up to 56 MHz can be generated on the transmitter board.

2.1.5 EEPROM

The APIX is configured with an EEPROM. After release of the APIX reset signal, APIX accesses the EEPROM to obtain the configuration data. To enable the µC to access the EEPROM and to program user-defined configuration data, the communication path from EEPROM to APIX and to the µC has to be multiplexed. This is handled by the PhotoMOS relay.

2.1.6 APIX

The APIX device is soldered onto the evaluation board. For reliability and performance reasons, no sockets are used. All APIX signals can be accessed via connectors which are arranged around the APIX device. Access to APIX signals is intended mainly for measurement purposes. If APIX signals need to be driven from an outside application, the CPLD, which drives the APIX signals by default, has to be tri-stated, for example, by changing the programming information. For detailed information, please contact the INOVA application support.

In addition, the PCB-to-PCB type connectors around APIX facilitate the mounting of a piggy-pack with an APIX socket.

2.1.7 Power Supply

The power supply system is fed through a 5.5V - 6.0V DC input. The RS232 power supply is separated from the power supply for the remaining board logic to prevent noise.

The board power supply is divided into 3 different power domains with a common ground system:

- VCCIO (3.3 Volt): CPLD, µC and APIX IOs
- VCCINT (1.8 Volt): APIX analog power supply
- VDD (1.8 Volt): APIX digital power supply

2.2 Transmitter Board (Details)

2.2.1 Layout of Connectors

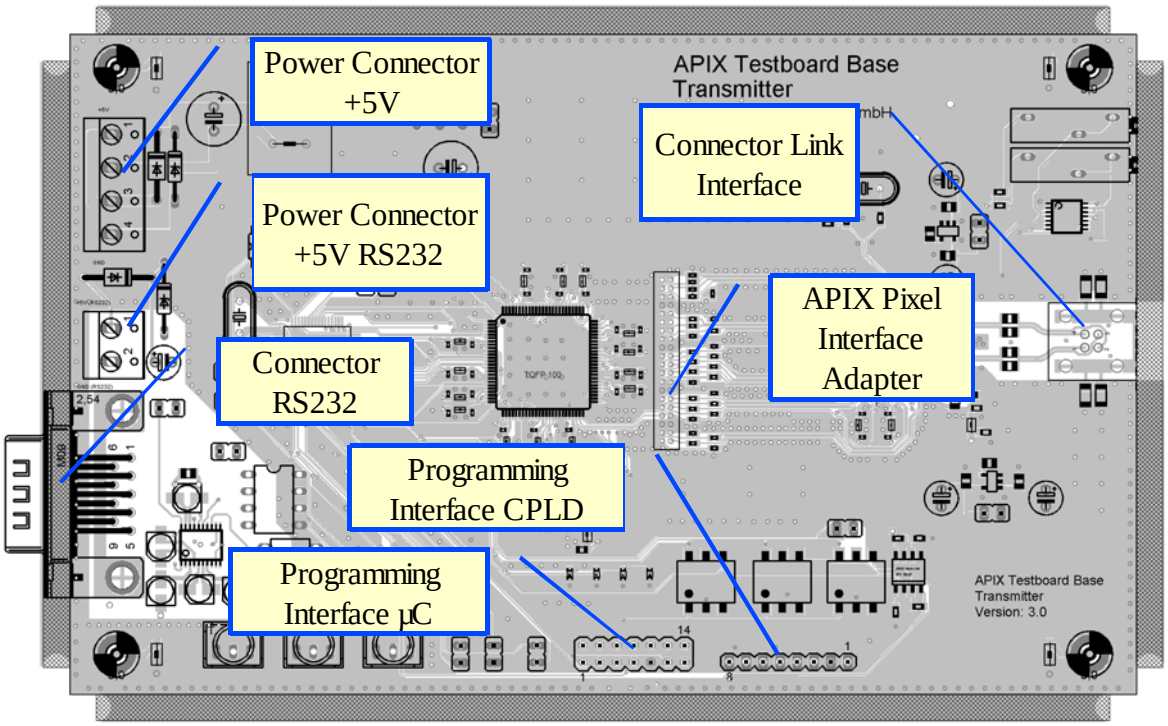

Figure 5: TX Board Connectors

2.2.2 Power Connector +5V

Pin No.	Signal	Type	Description
1	+5V	PWR	Power supply input (+5.6 V), a diode for reverse polarity protection is included.
2	GND	PWR	Ground
3	+5V	PWR	Internally connected to pin no. 1
4	GND	PWR	Internally connected to pin no. 2

Table 1: Power Connector +5V

2.2.3 Power Connector RS232

Pin No.	Signal	Type	Description
1	+5V (RS232)	PWR	Isolated input power supply (+5.6 V) of the RS232 interface. A diode for reverse polarity protection is included. The RS232 logic is optically decoupled from the rest of the design.
2	GND (RS232)	PWR	Isolated RS232 interface ground.

Table 2: Power Connector RS232

2.2.4 Connector RS232

Pin No.	Signal	Type	Description
1,5	GND (RS232)	PWR	GND of RS232 interface
2	RS232TX	OUT	TX signal of RS232
3	RS232RX	IN	RX signal of RS232
G1	RS232Shield		
G2	RS232Shield		

Table 3: Connector RS232

All other pins are not connected.

2.2.5 Programming Interface µC

Pin No.	Signal	Type	Description
1	UP_TC		
2	VCCIO	PWR	Power supply
3	UP_TMS		
5	UP_TDI		
7	UP_TDO_TDI		
9	GND	PWR	Ground
11	RST_NMI		

Table 4: Programming Interface µC

All other pins are not connected.

2.2.6 Programming Interface CPLD

Pin No.	Signal	Type	Description
1	TCK		Clock
2	GND	PWR	Ground
3	TMS		
6	TDI		Data input
7	TDO_TDI		Data out, Data in
8	VCCIO	PWR	Power supply

Table 5: Programming Interface CPLD

All other pins are not connected.

2.2.7 Connector Automotive Pixel Link Interface

Pin No.	Signal	Type	Description
2	SDIN-	I	Inverted signal of optional upstream link
3	SDOUT+	I/O	Non-inverted signal of downstream link
4	SDIN+	I	Non-inverted signal of optional upstream link

1	SDOUT-	I/O	Inverted signal of downstream link
	Shield		Connected to GND via RC combination
	Shield		Connected to GND via RC combination

Table 6: Connector Automotive Pixel Link Interface

2.2.8 APIX Pixel Interface Adapter (TX Side)

The APIX Pixel Interface adapter provides direct access to the APIX pixel interface. This enables the interfacing of any external, parallel pixel data source.

Providing data at the Pixel APIX Pixel Interface adapter requires a reprogramming of the CPLD to avoid multiple drivers (CPLD and external data source) on the APIX pixel bus! For further information please contact INOVA application support!

Pin No.	Signal	Type	Description
1	PLD_DE	IN	Pixel data enable
2	PLD_SBUP_DATA1	OUT	Upstream side band data bit 1
3	PLD_HS	IN	Pixel data horizontal synchronization signal
4	PLD_VS	IN	Pixel data vertical synchronization signal
5	PLD_PD15	IN	Pixel data bit 15
6	PLD_PD13	IN	Pixel data bit 13
7	GND	PWR	Signal ground
8	GND	PWR	Signal ground
9	PLD_PD10	IN	Pixel data bit 10
10	PLD_PD18	IN	Pixel data bit 18
11	PLD_SBDOWN_DATA 1	IN	Downstream side band data bit 1
12	PLD_SBDOWN_DATA 0	IN	Downstream side band data bit 0
13	PLD_PD0	IN	Pixel data bit 0
14	PLD_SBUP_DATA0	OUT	Upstream side band data bit 0
15	PLD_PD2	IN	Pixel data bit 2
16	PLD_PD1	IN	Pixel data bit 1
17	GND	PWR	Signal ground
18	GND	PWR	Signal ground
19	PLD_PD4	IN	Pixel data bit 4
20	PLD_PD3	IN	Pixel data bit 3
21	PLD_PD6	IN	Pixel data bit 6

22	PLD_PD5	IN	Pixel data bit 5
23	PLD_PD8	IN	Pixel data bit 8
24	PLD_PD7	IN	Pixel data bit 7
25	PLD_PCLK	IN	Pixel data clock
26	PLD_PD9	IN	Pixel data bit 9
27	GND	PWR	Signal ground
28	GND	PWR	Signal ground
29	PLD_PD19	IN	Pixel data bit 19
30	PLD_PD11	IN	Pixel data bit 11
31	PLD_PD21	IN	Pixel data bit 21
32	PLD_PD20	IN	Pixel data bit 20
33	PLD_PD14	IN	Pixel data bit 14
34	PLD_PD12	IN	Pixel data bit 12
35	GND	PWR	Signal ground
36	GND	PWR	Signal ground
37	PLD_PD22	IN	Pixel data bit 22
38	PLD_PD23	IN	Pixel data bit 23
39	PLD_PD16	IN	Pixel data bit 16
40	PLD_PD17	IN	Pixel data bit 17

Table 7: APIX Pixel Interface Adapter (TX Side)

2.2.9 Layout Control LEDs

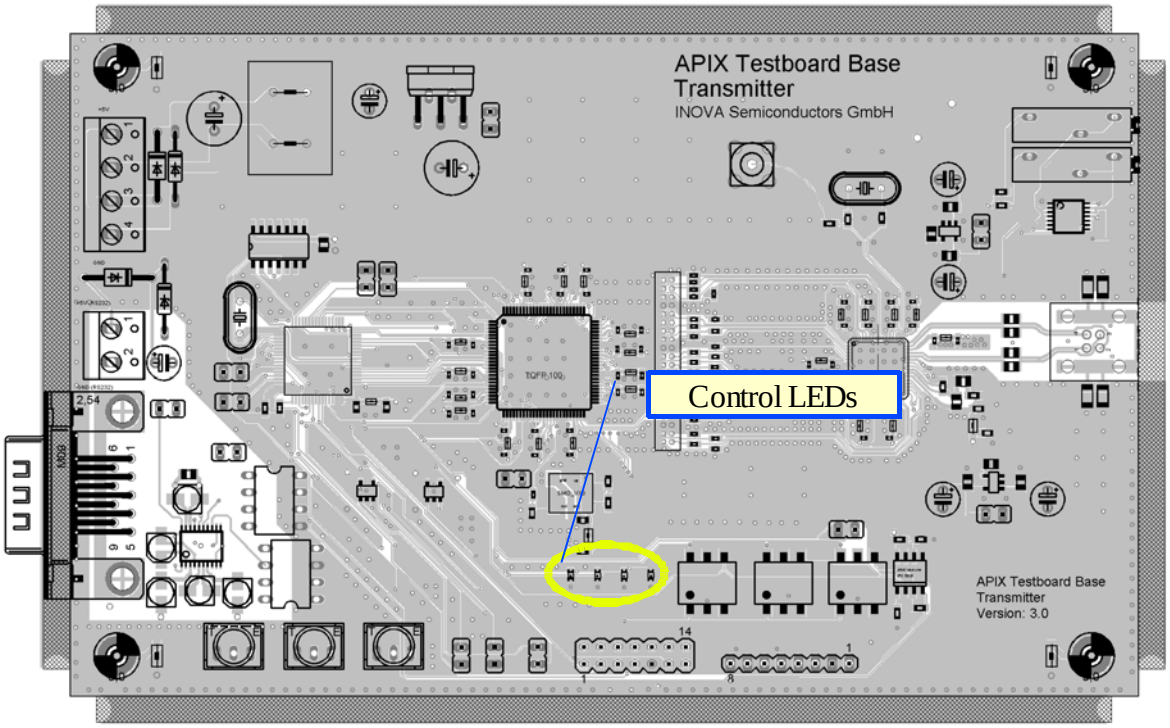

Figure 6: Layout of control LEDs

Part	Color	Signal	Description
LED1	Yellow	LED1	Configurable through operating SW (not used in default mode)
LED2	Green	LED2	Configurable through operating SW (default: LED is flashing during normal operation)
LED3	Red	Power up_Reset_P	LED is on during power-up
LED4	Red	APIX_Reset_P	LED is on during reset of APIX

Table 8: Control LEDs

2.2.10 Jumpers

Part Name	Signal 1	Signal 2	Description
EXTCLOCK	UC_CLK	GND	Optional external clock signal to CPLD
JP2	VCCINT	GND	Test point 1.8 Volt VDD (APIX)
JP3	VCCIO	GND	Test point 3.3 Volt VCCIO
JP4	VDD	GND	Test point 1.8 Volt VDDA (APIX)
JP7	GND	MR_UC	Set jumper to reset µC

JP9	GND	UC_RESETREQUEST	Set jumper to reset APIX and CPLD
JP10	POWERUP_RESET_N	RST_NMI	Remove jumper for flash programming of µC Set jumper to normal (reset) function of µC
JP13	MAX232SHDN#	GND1	Set jumper to shut-down of RS232 (e.g. for EMI tests)
JP14	TX_ERROR	GND	Test point TX_error signal
JP15	GND	PLD_GPIO1	Test point CPLD general purpose IO
JP16	GND	PLD_GPIO0	Test point CPLD general purpose IO
JP17	GND	CLOCKEXT	Optional clock input into CPLD
UART1	URXD1	UTXD1	UART connection of µC

Table 9: Jumpers

2.3 Receiver Board (Details)

2.3.1 Layout of Connectors

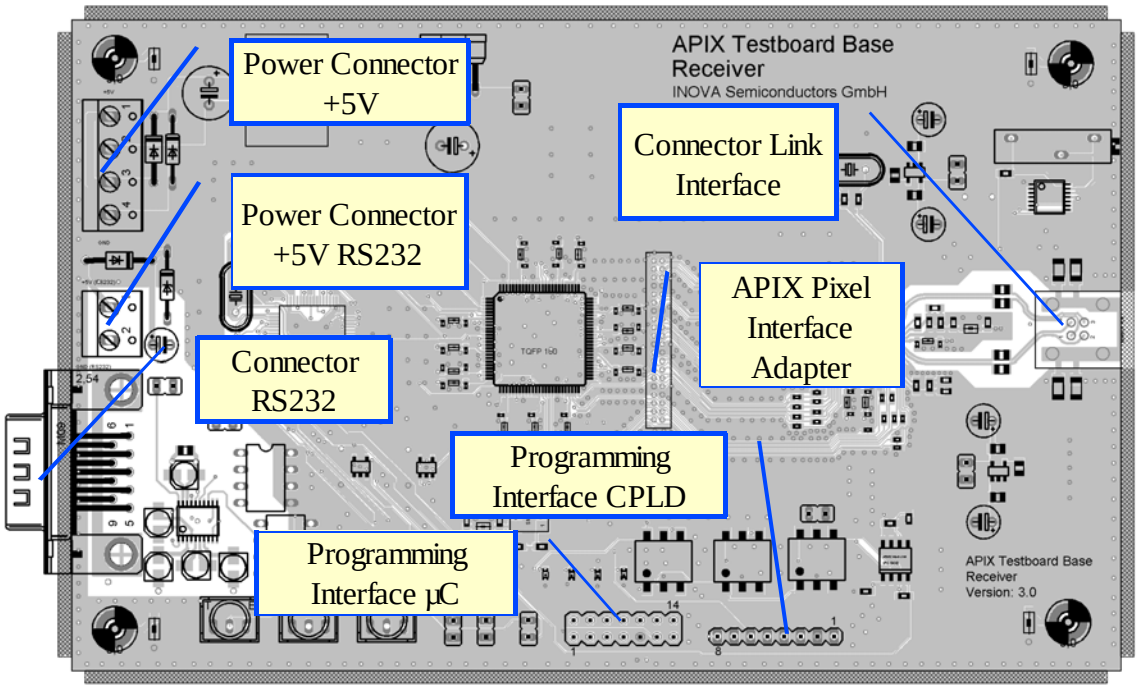

Table 10: RX Board Connectors

2.3.2 Power Connector +5 V

Pin No.	Signal	Type	Description
1/5	+5V	PWR	Power supply input (+5.6 V), a diode for reverse polarity protection is included.
2	GND	PWR	Ground
3	+5V	PWR	Internally connected to pin no. 1
4	GND	PWR	Internally connected to pin no. 2

Table 11: Power Connector +5V

2.3.3 Power Connector RS232

Pin No.	Signal	Type	Description
1	+5V (RS232)	PWR	Isolated input power supply (+5.6 V) of the RS232 interface. A diode for reverse polarity protection is included. The RS232 logic is optically decoupled from the rest of the design.
2	GND (RS232)	PWR	Isolated RS232 interface ground.

Table 12: Power Connector RS232

2.3.4 Connector RS232

Pin No.	Signal	Type	Description
1	GND (RS232)	PWR	GND of RS232 interface
2	RS232TX	OUT	TX signal of RS232
3	RS232RX	IN	RX signal of RS232
G1	RS232Shield		
G2	RS232Shield		

Table 13: Connector RS232

All other pins are not connected.

2.3.5 Programming Interface µC

Pin No.	Signal	Type	Description
1	UP_TCK		
2	VCCIO	PWR	Power
3	UP_TMS		
5	UP_TDI		
7	UP_TDO_TDI		
9	GND	PWR	Ground
11	RST_NMI		

Table 14: Programming Interface µC

All other pins are not connected.

2.3.6 Programming Interface CPLD

Pin No.	Signal	Type	Description
1	TCK		
2	GND	PWR	Ground
3	TMS		
6	TDI		
7	TDO_TDI		
8	VCCIO	PWR	Power Supply

Table 15: Programming Interface CPLD

All other pins are not connected.

2.3.7 Connector Automotive Pixel Link Interface

Pin No.	Signal	Type	Description
3	SDOUT-	OUT	Inverted signal of optional upstream link
2	SDIN+	I/O	Non-inverted signal of downstream link
1	SDOUT+	OUT	Non-inverted signal of optional upstream link
4	SDIN-	I/O	Inverted signal of downstream link
	Shield		Connected to GND via RC combination
	Shield		Connected to GND via RC combination

Table 16: Connector Automotive Pixel Link Interface

2.3.8 APIX Pixel Interface Adapter (Rx Side)

Pin No.	Signal	Type	Description
1	SBUP_D0	IN	Upstream side band data bit 0
2	SBUP_D1	IN	Upstream side band data bit 1
3	PLD_SBDOWN_CK	OUT	Downstream side band data clock
4	PLD_PD18	OUT	Pixel data bit 18
5	PLD_PD19	OUT	Pixel data bit 19
6	PLD_PD20	OUT	Pixel data bit 20
7	GND	PWR	Signal ground
8	GND	PWR	Signal ground
9	PLD_PD10	OUT	Pixel data bit 10
10	PLD_PD0	OUT	Pixel data bit 0
11	PLD_PD1	OUT	Pixel data bit 1
12	PLD_PD2	OUT	Pixel data bit 2
13	GND	PWR	Signal ground
14	GND	PWR	Signal ground
15	PLD_PD3	OUT	Pixel data bit 3

16	PLD_PD4	OUT	Pixel data bit 4
17	PLD_PD5	OUT	Pixel data bit 5
18	PLD_PD6	OUT	Pixel data bit 6
19	PLD_PD7	OUT	Pixel data bit 7
20	PLD_PD8	OUT	Pixel data bit 8
21	PLD_PD9	OUT	Pixel data bit 9
22	GND	PWR	Signal ground
23	GND	PWR	Signal ground
24	PLD_PD11	OUT	Pixel data bit 11
25	PLD_PD12	OUT	Pixel data bit 12
26	PLD_PD13	OUT	Pixel data bit 13
27	PLD_PD14	OUT	Pixel data bit 14
28	PLD_PD15	OUT	Pixel data bit 15
29	PLD_DE	OUT	Pixel data enable
30	PLD_VS	OUT	Pixel data vertical synchronization signal
31	PLD_HS	OUT	Pixel data horizontal synchronization signal
32	GND	PWR	Signal ground
33	GND	PWR	Signal ground
34	PLD_PCLK	OUT	Pixel data clock
35	PLD_SBDOWN_D0	OUT	Downstream side band data bit 0
36	PLD_PD16	OUT	Pixel data bit 16
37	PLD_PD17	OUT	Pixel data bit 17
38	PLD_PD21	OUT	Pixel data bit 21
39	PLD_PD22	OUT	Pixel data bit 22
40	PLD_PD23	OUT	Pixel data bit 23

2.3.9 Layout of Control LEDs

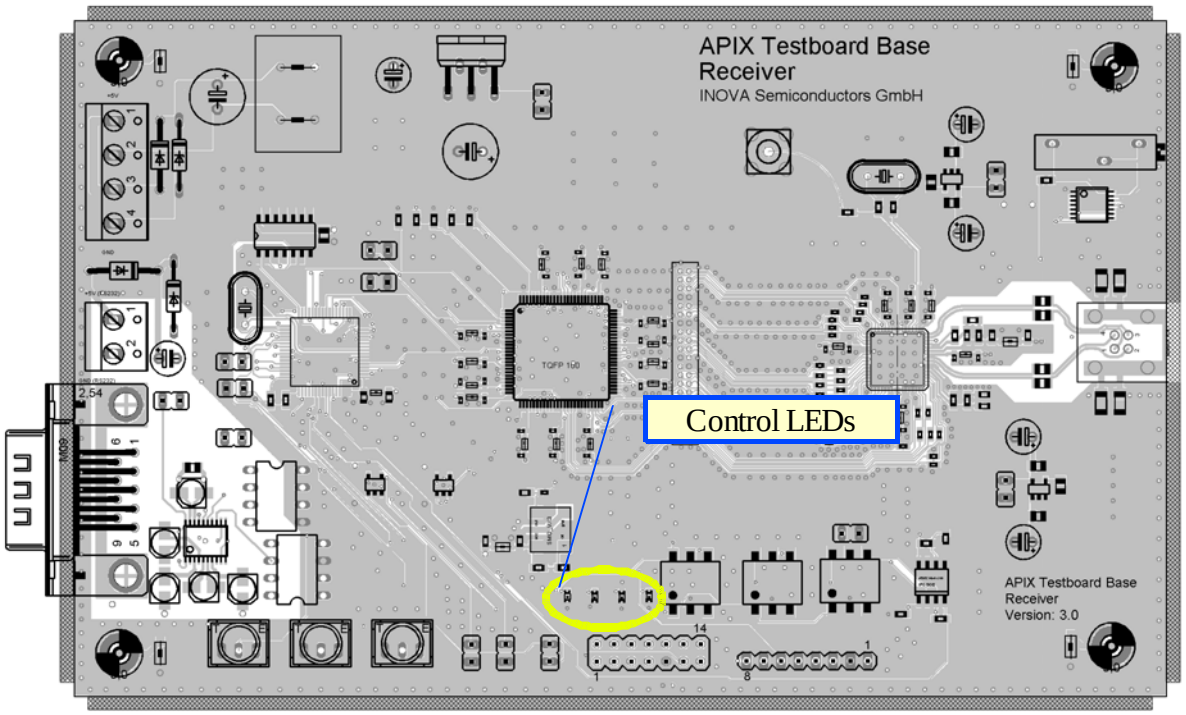

Figure 7: Layout of RX Board Buttons and LEDs

Part	Color	Signal	Description
LED1	Yellow	LED1	Configurable through operating SW (not used in default mode)
LED2	Green	LED2	Configurable through operating SW (default: LED is flashing during normal operation)
LED3	Red	Powerup_Reset_P	LED is on during power-up
LED4	Red	APIX_Reset_P	LED is on during reset of APIX

Table 17: Control LED's

2.3.10 Jumpers

Part Name	Signal 1	Signal 2	Description
EXTCLOCK	UC_CLK	GND	Optional external clock signal to CPLD
JP2	VCCINT	GND	Test point 1,.8 Volt VDD (APIX)
JP3	VCCIO	GND	Test point 3.3 Volt VCCIO
JP4	VDD	GND	Test point 1.8 Volt VDDA (APIX)
JP7	GND	MR_UC	Set jumper to reset µC

JP9	GND	UC_RESETREQUEST	Set jumper to reset APIX and CPLD
JP10	POWERUP_RESET_N	RST_NMI	Remove jumper for flash programming of µC Set jumper for normal (reset) function of µC
JP13	MAX232SHDN#	GND1	Set jumper to shut-down of RS232
JP14	GND	RX_ERROR	Test point RX_error signal
JP15	GND	PLD_GPIO0	Test point CPLD general purpose IO
JP16	GND	PLD_GPIO1	Test point CPLD general purpose IO
UART1	RX	TX	UART Connection of µC

Table 18: Jumpers

2.4 Powering up the Evaluation Kit

- Check jumper settings first:

TX Jumper	Setting	Rx Jumper	Setting
EXTCLOCK	off	EXTCLOCK	off
JP2	off	JP2	off
JP3	off	JP3	off
JP4	off	JP4	off
JP7	off	JP7	off
JP8	off	JP8	off
JP9	off	JP9	off
JP10	on	JP10	on
JP13	off	JP13	off
JP14	off	JP14	off
JP15	off	JP15	off
JP16	off	JP16	off
JP17	off	JP17	off
UART	off	UART	off

Table 19: Jumper settings for power up

- Connect transmitter and receiver board with the provided 5 m quad STP cable (connector link interface).

- Connect PC/laptop COM1 and COM2 ports with RS232 connector via the provided RS232 cable.

- Provide +5.6 V power supply to power connector +5 V (1) and power connector +5 V RS232 (2). Power supply needs to higher than 5.0V to compensate the voltage drop across the reverse polarity protection diodes.

- Start the GUI as described in Section 3
- Check EEPROM settings. By default the Windows GUI reads the EEPROM settings from the boards.
- Set the Equalizer setting to: Off in RX EEPROM menu. The provided cable does not require the equalizer. Enabling the equalizer causes overcompensation, what leads to bit errors.
- Disable the Wobble feature in TX EEPROM menu at the beginning. If the wobble feature is enabled the eye opening is reduced and might cause an increased bit-error rate.

3.0 Graphical User Interface

The graphical user interface interacts with the evaluation boards through the serial port connections. The software allows to configure the INAP125T or INAP125R registers and to control the resistor values for pre-emphasis and nominal current. In addition, the software offers the ability to download and verify the transmission of different test patterns for video and sideband communication.

3.1 Installation

3.1.1 Requirements

Operation System Requirements:

- Windows XP 32-bit
- Windows Vista 32-bit

Communication interface:

- Minimum 1 Serial port, 2 ports required for full evaluation

3.1.2 Installation

Please follow the installation procedure of the CD. The program will be accessible through “Start/Programs/Inova Semiconductors/APIXEval”.

3.1.3 Preparation

The Evaluation Software requires the serial ports of the evaluation kits to be connected to the PC. Please connect the evaluation kits with the null modem cable to the serial port of the PC and power up the boards. Afterwards please start the software.

The software will remember the board setup for the next start. Therefore, please make sure that the boards are connected and powered before starting the software. If a board is connected or powered up after the software has been started, please use the option menu as described in Section 3.2.2 to retrigger the initialization.

3.2 Concept and general usage

The Graphical user interface is split into 2 main parts: the configuration section and the status section.

The Configuration section is separated into different configuration tabs:

- Downstream
- Upstream
- Options (various options for TX and RX, not directly related to the APIX link)
- Physical layer (Pre-emphasis and nominal current control)
- Video generation (Test pattern generator for the video interface)
- Sideband generation (Test pattern generator for the sideband interfaces)

On each configuration, except the test pattern generators, transmitter settings are listed at the left side, receiver settings on the right side.

The Status section reflects the real-time status of the evaluation boards and the test pattern generation and verification.

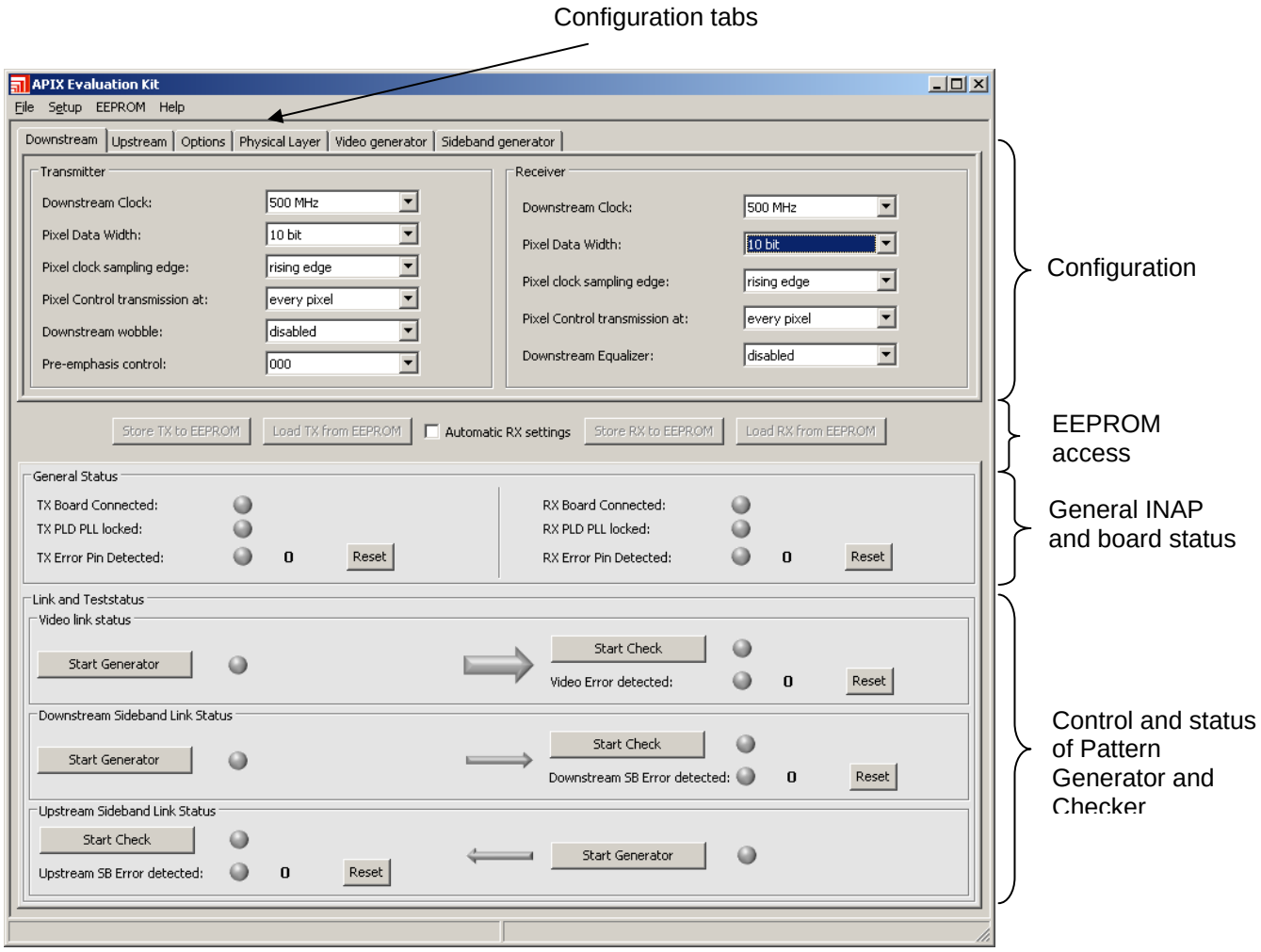

Figure 8: APIX Evaluation Software Overview

3.2.1 Software Configuration

By default on first boot-up, the software needs to be configured to the correct Serial ports, in order to set the communication with the evaluation boards. If no port has been configured the software will automatically bring up the options dialog, which can be found in the menu under “Setup/Options”.

The UART communication tab offers two drop-down boxes to select the correct serial ports to be used.

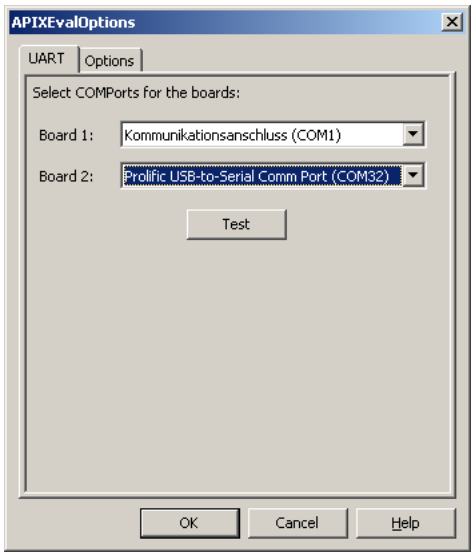

Figure 9: UART configuration

The Test button allows to trigger a ‘Ping’ to the evaluation board. The boards should respond with one of the following messages (the COM port displayed depends on your selection).

Figure 10: TX Board detected

Figure 11: RX Board detected

The second tab “Options” offers different settings for the use of the software:

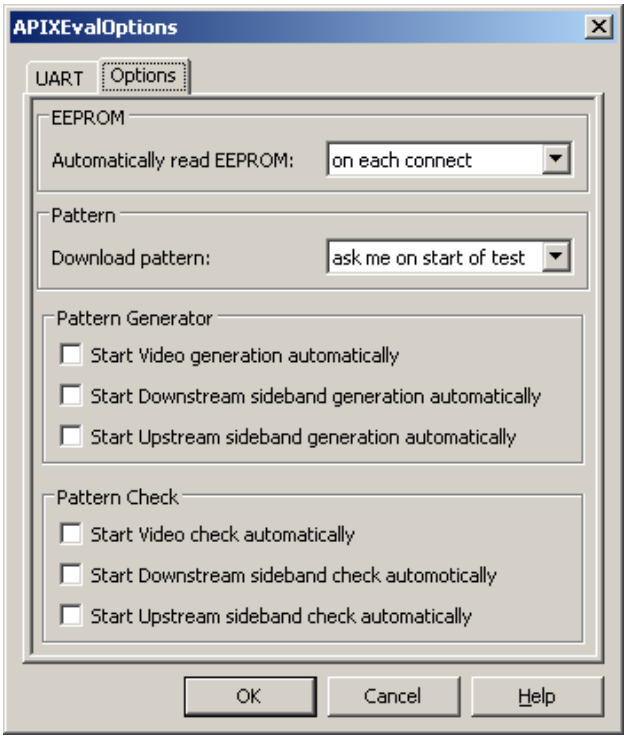

Figure 12: Configuration options

Category	Setting	Description
EEPROM	Automatically read EEPROM: - on each connect - never	By default, the software reads the actual EEPROM settings, if a board has been detected or on software start.
Pattern	Download pattern: - manually - automatically - ask me on start of test	Video, downstream and upstream test patterns need to be downloaded to the board CPLD of transmitter and receiver. In order to ensure, that the same pattern is downloaded, the software acts according to this setting if a board has been detected.
Pattern generator	Start Video, Downstream or upstream generation automatically	While enabled, the software starts the respective generator as soon as a board is detected. The generator might require to download a pattern before use.
Pattern checker	Start Video, Downstream or upstream checker automatically	While enabled, the software starts the respective checker on the CPLD as soon as a board is detected. The checker might require to download the pattern before use.

Table 20: User Interface Options

3.2.2 Board Status

The board status is displayed in the lower part of the dialog in section “General status”. The LEDs indicate the status of the board.

Figure 13: Board status, no board connected

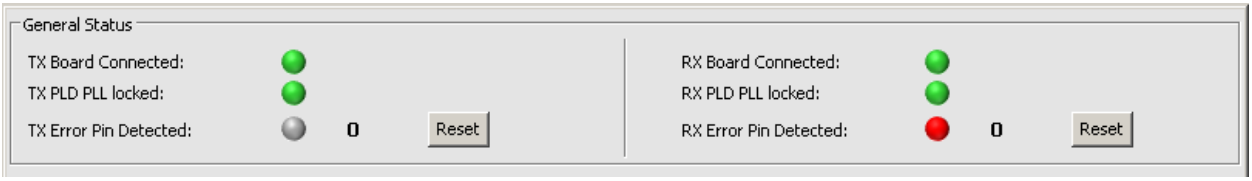

Figure 14: Board status, TX and RX board connected

Status	Indicator	Description
TX/RX Board connected	Grey	No board detected, check UART connection or try to restart transmission by opening and confirming the options dialog.
TX/RX Board connected	Green	UART connection to board established, ready to accept commands. This is mandatory for all other indicators.
TX/RX PLD locked	Grey	Board PLD, which is required for pattern test and check is not locked. Please verify clock source if external clock is used or switch to predefined clock.
TX/RX PLD locked	Green	Board PLD locked
TX/RX Error pin Detected	Grey	Error pin is low. No Error indicated
TX/RX Error pin Detected	Red	Error pin is high. Indicates the Status as configured by the register setting for the Error pin (see ##).

Table 21: General status indicators

The counter after TX Error pin and RX Error pin shows indicates the number of rising edges detected at the pin, which can be Reset to 0 using the respective button.

By default, the evaluation boards come up with the default configuration of INAP125T and INAP125R. If both boards are connected and wired up correctly, the status of the boards should be indicated as shown in Figure 14. The RX Error pin indicates, that no correct video link is detected (only possible with a video stream applied to the pixel interface at the transmitter, see Section 3.2.4).

Since the upstream is enabled by default, the TX Error pin should stay grey which indicates “Upstream locked”.

3.2.3 INAP125 Configuration

In order to configure the device registers and the serial interface, the software offers several configuration tabs. The tabs for the configuration of the INAP125 registers are

- Downstream
- Upstream
- Options

Each tab is split into settings for the transmitter at the left part and the receiver at the right part of the interface. Since some of the parameters need to be equal on TX and RX for a successful link, the software offers the “automatic RX settings” feature, which automatically adjusts the RX settings to the TX settings. The Automatic RX settings can be enabled or disabled using the check box underneath the settings tabs.

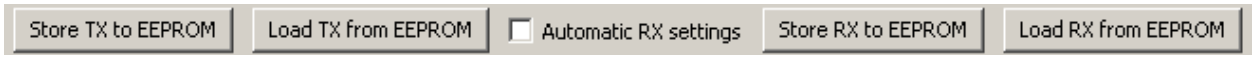

Figure 15: Buttons for Store and Load with checkbox for automatic RX settings

The buttons for loading or storing the EEPROM are enabled as soon as the board status might not meet the settings in the software. After a load or store operation, the buttons are disabled, to indicate, that the status matches the board EEPROM.

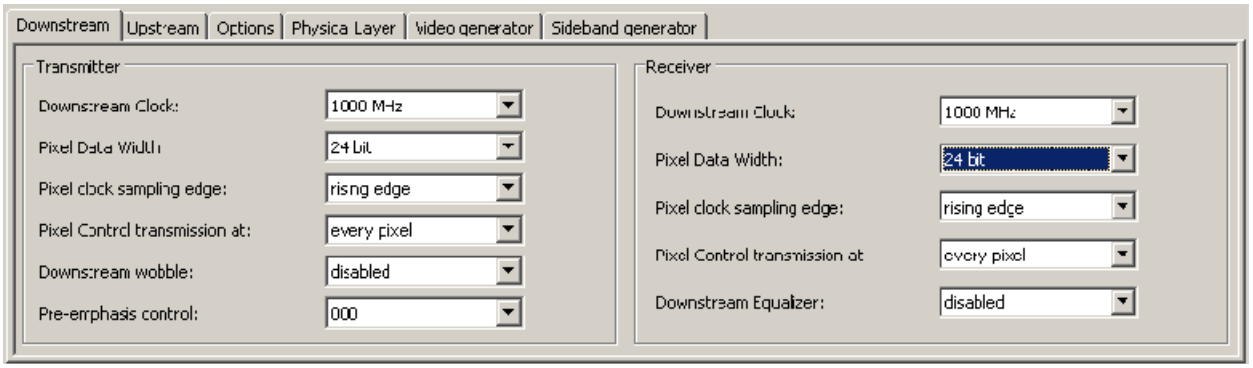

Figure 16: Downstream configuration

Item	Options	Description
Downstream clock	500 MHz 1000 MHz	High speed serial line clock. The setting must be equal on TX and RX.
Pixel data width	10 bit 12 bit 18 bit 24 bit	Configures the pixel data interface PX_DATA at TX and RX. The setting must be equal on TX and RX. The pixel width has also influence on the maximum pixel clock possible at the serial link. Please see datasheet for more information.
Pixel clock sampling edge	falling edge rising edge	Defines the sampling edge of the pixel data interface. The setting is local to TX and RX and does not have to be equal.
Pixel control transmission	never even pixels every pixel	Defines, how often the Pixel control data at PX_CTRL are sent over the serial line. The setting must be equal on TX an RX.
Downstream wobble (TX)	disabled enabled	Additional spread spectrum jitter on the serial line. The setting is typically not required and recommended to be disabled. Enabling wobbling decreases the signal quality and therefore maximum range

		and bit error rate of the APIX link
Pre-emphasis control (TX)	000 – 111	Selects the amount of consecutive, equal polarity serial bits required to trigger the pre-emphasis current
Downstream Equalizer (RX)	disabled enabled	The downstream equalizer “amplifies” the received signal, in order to reach longer cable length. Since the equalizer also amplifies “noise”, typically better results can be achieved by tuning nominal current and pre-emphasis at the transmitter.

Table 22: Downstream configuration

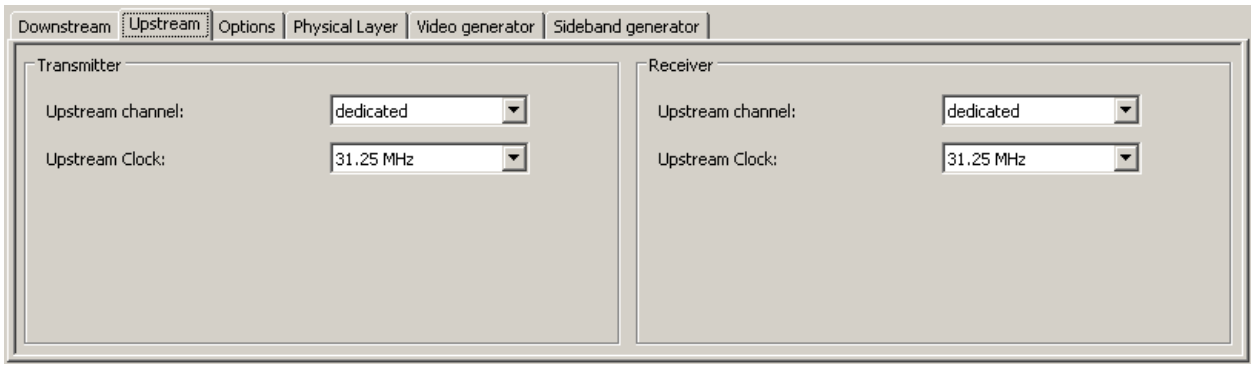

Figure 17: Upstream Configuration

Item	Options	Description
Upstream channel	Disabled embedded dedicated	Configures the upstream channel transmission. The settings must be equal on TX and RX.
Upstream Clock	20.83 MHz 31.25 MHz 41.67 MHz 62.5 MHz	The upstream clock defines the serial line clock used for the upstream channel. The selection options depend on the downstream clock selected (see Table 21: Downstream configuration). The upstream clock must be equal on TX and RX.

Table 23: Upstream configuration

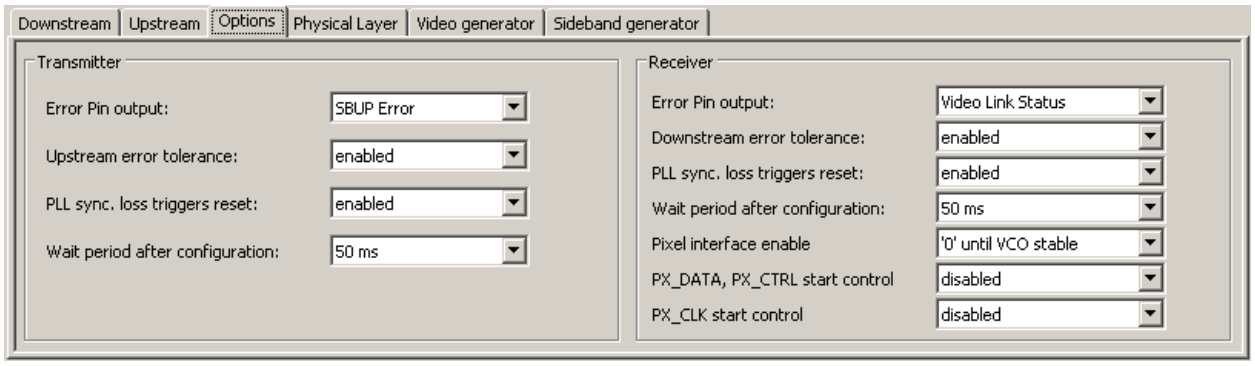

Figure 18: Option Configuration

Item (TX)	Options	Description
Error pin output	SBUP Error	The Error pin is high (LED Red) when the upstream is not enabled or an error has been detected
	SBUP Restart	The Error pin is high (LED Red) when the upstream has been restarted
Upstream error tolerance	disabled enabled	If enabled a single frame error does not trigger the TX error signal. It is triggered if a 2nd error is detected within the next 7 frames.
PLL synchronization loss triggers reset	disabled enabled	If enabled, the device performs a reset on synchronization loss of the internal PLL
Wait period after configuration	Disabled 50 ms	Introduces a 50ms delay after reset before transmission start, e.g. to settle the PLL.

Table 24: Transmitter Options configuration

Item (RX)	Options	Description
Error pin output	Video Link Status	High indicates an error on either the downstream link or the video transmission
	Pixel Clock status	Low indicates a successful lock on the pixel clock
	Link Established	High indicates that the serial link is established
	CTRL2 detected	High indicates that the pixel interface is synchronized to the video timing
	Pixel buffer error	High indicates that pixel buffer is full or empty
Downstream error tolerance	disabled enabled	If enabled a single frame error does not trigger the RX error signal. It is triggered if a 2nd error is detected within the next 7 frames.
PLL synchronization loss triggers reset	disabled enabled	If enabled, the device performs a reset on synchronization loss of the internal PLL
Wait period after configuration	Disabled 50 ms	Introduces a 50ms delay after reset before transmission start, e.g. to settle the PLL.
Pixel clock enable	'0' until VCO stable always enabled	The setting controls the behavior of the pixel clock output, which can be forced to low until receiver clock recovery is locked to the received pixel clock.
PX_DATA, PX_CTRL start control	Disabled start at upper left corner	If enabled, the INAP125R starts PX_DATA and PX_CTRL at the upper left corner.
PX_CLK start control	Disabled start at upper left corner	If enabled, the INAP125R starts the PX_CLK at the upper left corner of the display.

Table 25: Receiver Options configuration

The tab to configure the nominal current and pre-emphasis is called "Physical layer".

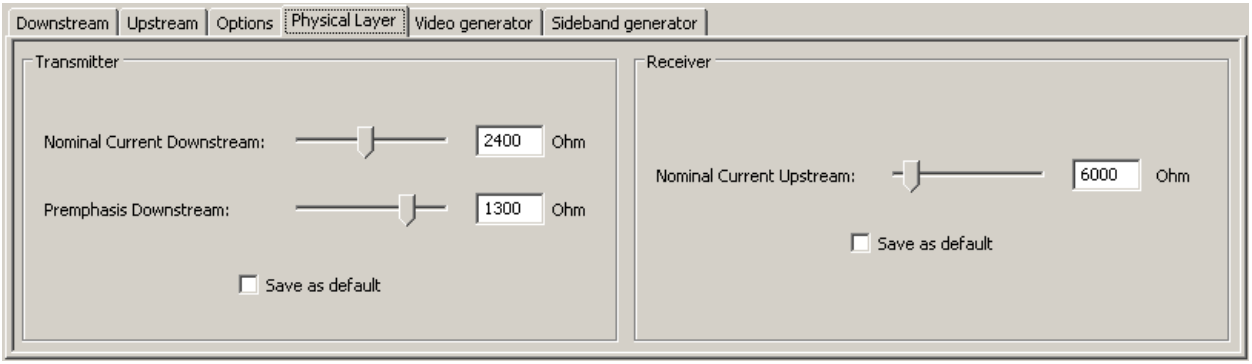

Figure 19: Physical Layer configuration

The different sliders allow to adjust the external resistor applied to the PRE_EMPH and NOM_CUR pins of the INAP125T and INAP125R. The value in the text box at the right of each slider represents the estimated resistor value. The adjustment of the value may be done either by moving the slider or by typing a value directly into the textbox. The minimum value for the resistor is 700Ohm, the maximum is 10000Ohm.

NOTE: The resistor may only be used as indicator for the final value required in the application. The resistor value may vary with different cables types, cable lengths, process variations and temperature.

3.2.4 Video test-pattern generation and check

The onboard CPLD of the APIX evaluation kit is able to generate and verify test patterns, transmitted over the APIX link.

The configuration tab “Video generator” offers various settings, to generate a realistic video stream, with various test-patterns and frequency. The pixel clock frequency may be generated by the CPLD, but may also be fed in externally to the CPLD. Once the pattern is defined, the pattern needs to be downloaded to the transmitter and the receiver devices for a successful verification using the “Download pattern” button. In case the button is disabled, the pattern has already been downloaded to the boards.

Depending on the options setting (see 3.2.1) the pattern may automatically be downloaded as soon as the checker or generator is restarted.

If you would like the selected pattern to be stored as default pattern for the next start of the software, please check the “save as default” checkbox.

If only one board is connected to the software, please make sure the remote device uses the same pattern as the one locally connected. Otherwise the checker may not be able to synchronize to the pattern and to detect bit errors.

NOTE: The generated pattern sent over the APIX is formed out a synchronization pattern between the CPLDs and the video pattern itself. Therefore the pattern might not generate a proper image at a display.

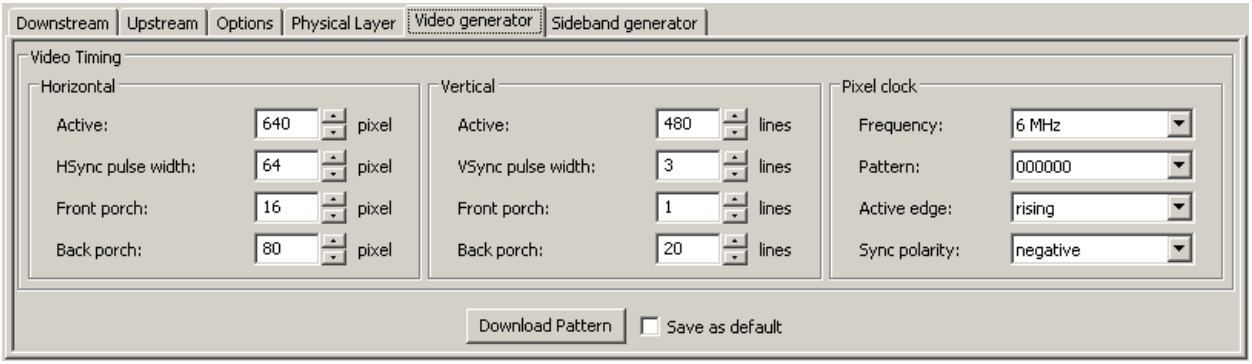

Figure 20: Video pattern configuration

Figure 21: Video test status

The status of the video test pattern can be verified in the status section of the user interface. To start the pattern generator at the transmitter, please use the “Start Generator” button. The status of the generator is indicated by the LED right next to the button. The arrow between TX and RX switches to green, when both TX and RX are connected to the same evaluation software and if generator and checker are activated.

Button name	Indicator	Description
“Start Generator”	Grey	Pattern generation stopped.
“Stop Generator	Green	Pattern generation started.

Table 26: Video generator LED status

Button name	Indicator	Description
“Start Check”	Grey	Pattern checker stopped.
“Stop Check	Yellow	Pattern checker started, but not synchronized to incoming pattern.
	Green	Pattern checker started and synchronized to incoming pattern.

Table 27: Video checker LED status

Status	Indicator	Description
Video Error detected	Grey	No errors detected
	Red	Bit error detected in video stream, amount indicated after LED

Table 28: Video Error status indicator

3.2.5 Sideband generator and checker

The sideband test pattern can be configured using the “Sideband pattern” tab.

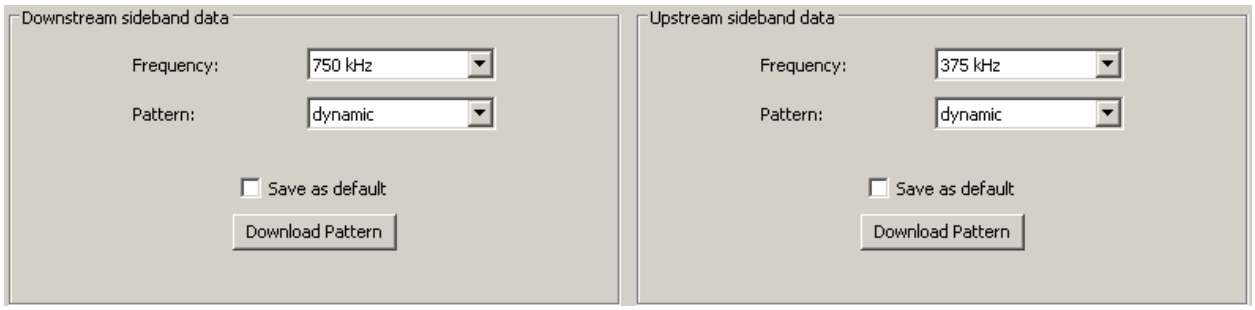

Figure 22: Downstream/Upstream test pattern configuration

The dialog offers the following options for the pattern.

Item (Downstream)	Options	Description
Frequency	750 kHz	Configures the pattern frequency, generated by the CPLD.
	1.5 MHz	Configures the pattern frequency, generated by the CPLD. This option is only available in 1000 MBit mode.
	External	Configures the CPLD to use the reference frequency applied to the input
Pattern	00 01 10 11	Stable pattern on the two sideband pins. The CPLD will also send a synchronization header.
	Dynamic	Dynamically alternates the pattern between 01 and 10. The CPLD also sends and expects a synchronization header.

Table 29: Downstream test pattern configuration

Item (Upstream)	Options	Description
Frequency	375 kHz 750 kHz	Configures the pattern frequency, generated by the CPLD
	External	Configures the CPLD to use the reference frequency applied to the input
Pattern	00 01 10 11	Stable pattern on the two sideband pins. The CPLD also sends and expects a synchronization header.
	Dynamic	Dynamically alternates the pattern between 01 and 10. The CPLD also sends and expects a synchronization header.

Table 30: Upstream test pattern configuration

The status of the downstream and upstream test pattern can be verified in the status section of the window. To start the pattern generators, please use the “Start Generator” button in the respective section. The status of the generator is indicated by the LED right next to the button. The arrow between TX and RX switches to green, when both TX and RX are connected to the evaluation software and if generator and checker are activated.

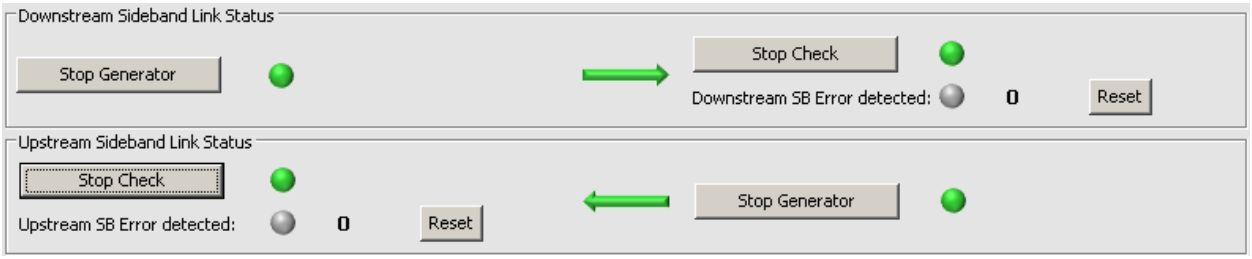

Figure 23: Downstream/Upstream test status

Button name	Indicator	Description
“Start Generator”	Grey	Pattern generation stopped.
“Stop Generator	Green	Pattern generation started.

Table 31: Downstream/upstream generator LED status

Button name	Indicator	Description
“Start Check”	Grey	Pattern checker stopped.
“Stop Check	Yellow	Pattern checker started, but not synchronized to incoming pattern.
	Green	Pattern checker started and synchronized to incoming pattern.

Table 32: Downstream/upstream checker LED status

Status	Indicator	Description
Downstream SB Error detected	Grey	No errors detected
	Red	Bit error detected in downstream sideband data stream, counter indicated after LED
Upstream SB Error detected	Grey	No errors detected
	Red	Bit error detected in upstream sideband data stream, counter indicated after LED.

Table 33: Video Error status indicator

4.0 Operating Conditions

- The board is designed to be used in a laboratory environment only.
- The maximum operating conditions may not be exceeded at any time.
- Precautions have to be taken against exposure of device terminals to electrostatic discharge stress.
- This board is designed for the purpose of electrical evaluation in an engineering environment and has not been EME-shielded. It must not be used in an environment where its electromagnetic emissions could impact the functions of other systems.
- The voltage supply should be properly filtered to avoid a deterioration of the bit error rate due to supply voltage spikes.
- It may be used within normal commercial temperature and humidity ranges.

4.1 Maximum Operating Conditions

Parameter	min.	max.	Unit
Temperature	0	35	°C
Humidity	0	90	%
Supply at Power Connector +5V	5.5	6.0	V
Supply at Power Connector +5V RS232	5.5	6.0	V

5.0 Mechanical Drawings

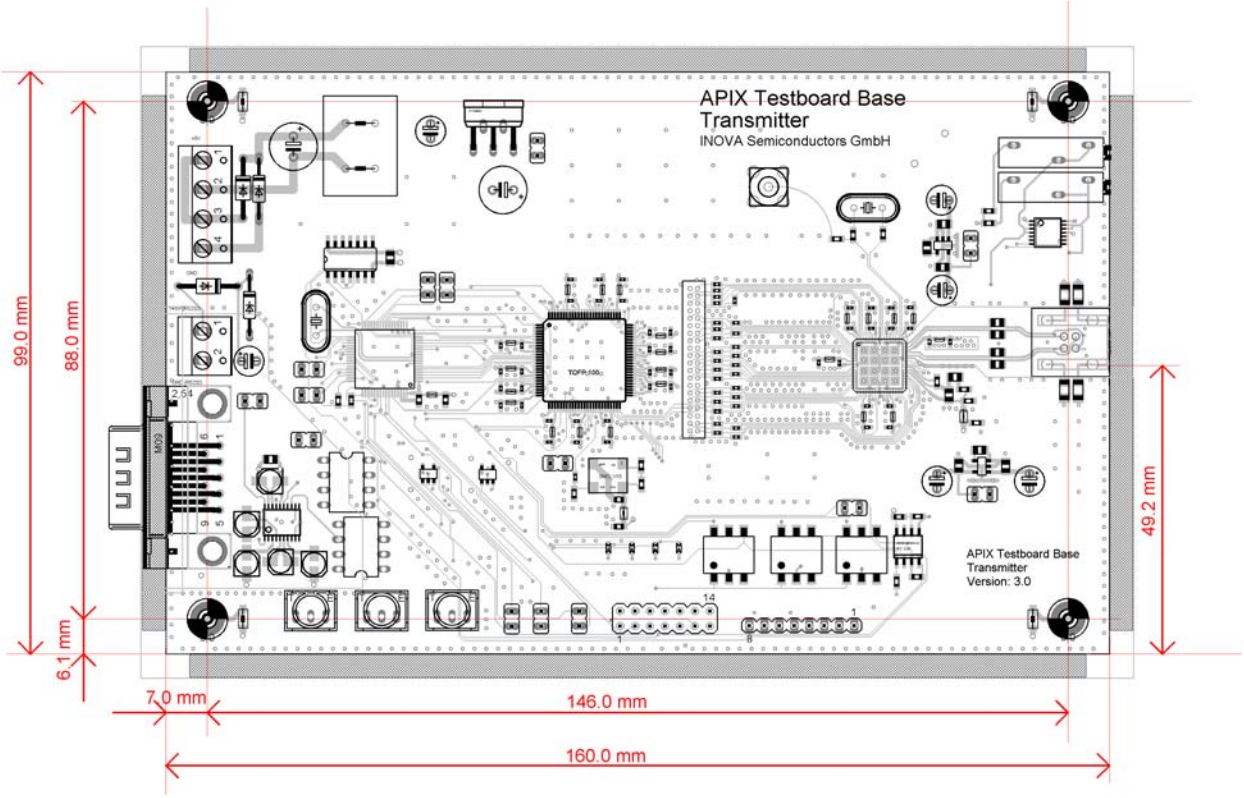

Figure 24: TX Board Dimensions

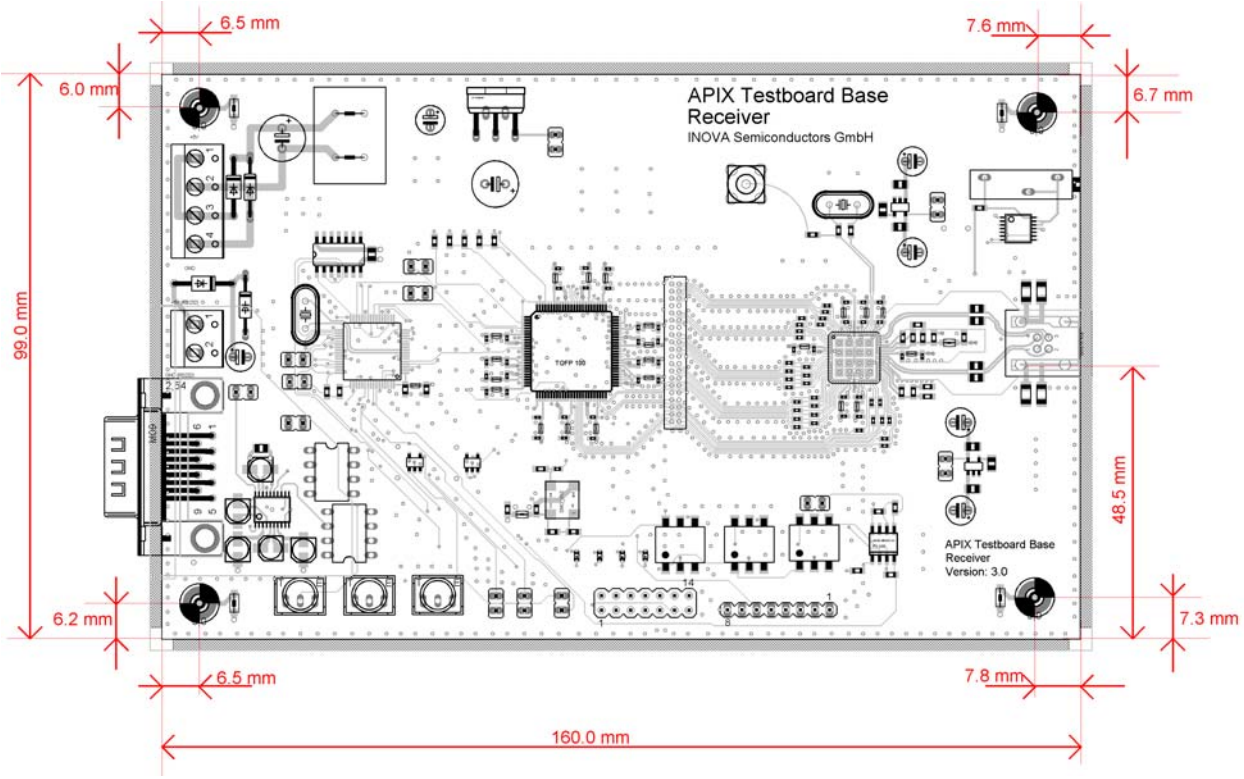

Figure 25: RX Board Dimensions

6.0 Additional Information

6.1 Ordering Code

Order the APIX Evaluation Kit (Board Revision 3.0) as: APIX_EVK

6.2 Further Documentation

- Schematics of the Evaluation Kit
- INAP125T and INAP125R data sheets
- AN100: Video interface application note
- AN101: Sideband configuration application note

6.3 Revision History

Version 1.0 (for Board Revision 3.0)

Version 1.1 (update GUI change)

Version 1.2 (update for Windows based Graphical User Interface)

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